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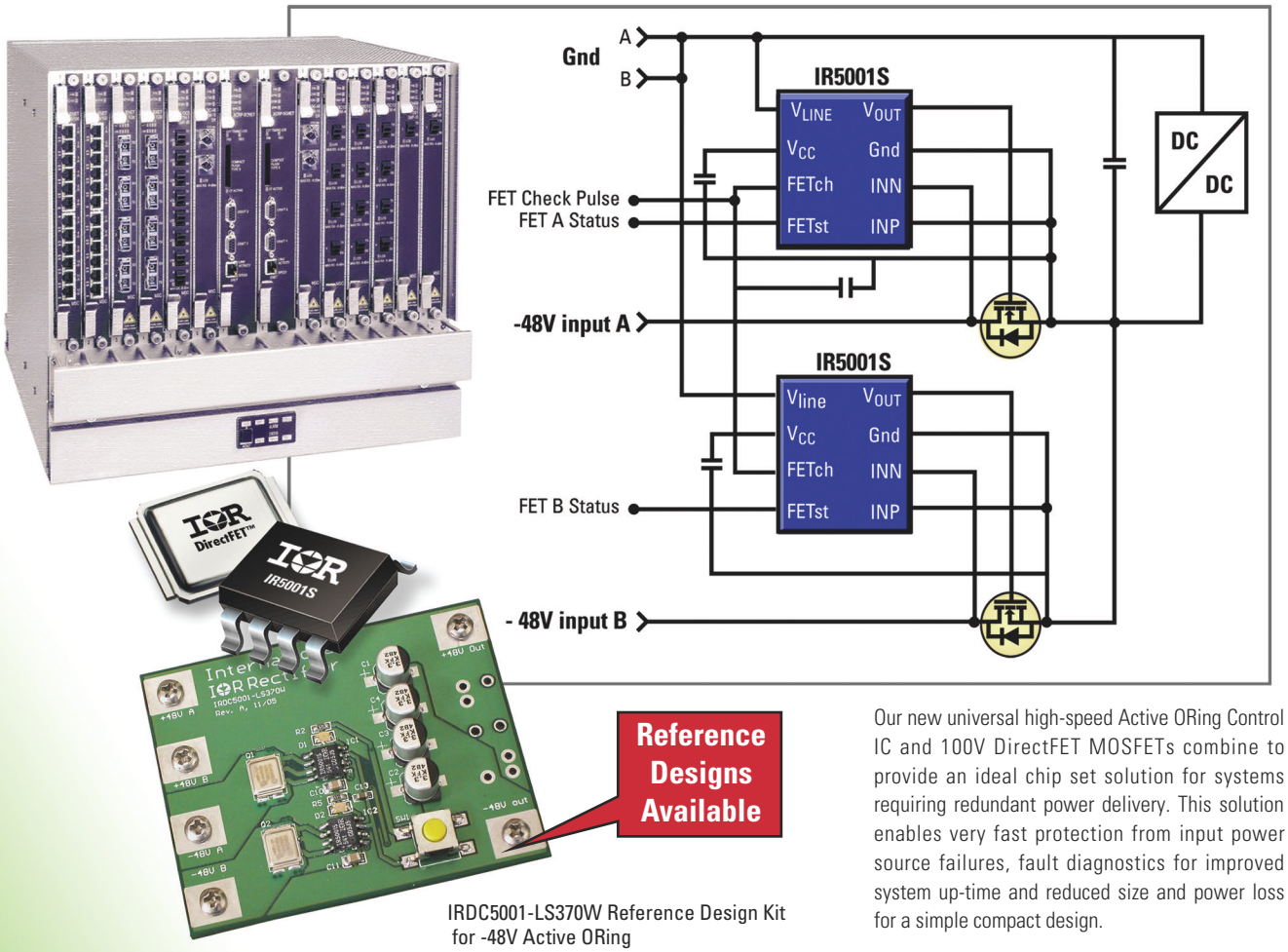

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* 100% tested and guaranteed over full temperature range

ACTIVE ORing DirectFET™ SELECTOR GUIDE

Part Number	Voltage	Package	$R_{DS(on)}$ max. @ $10V_{GS}$	Recommended Power Level for -48V System
IRF6644	100V	M-Can DirectFET	13mΩ	180W to 370W
IRF6662	100V	M-Can DirectFET	22mΩ	100W to 200W
IRF6645	100V	S-Can DirectFET	35mΩ	70W to 140W
IRF6655	100V	S-Can DirectFET	62mΩ	40W to 80W

IR's proprietary DirectFET technology is covered by US Patent 6,624,522 and other US and foreign pending patent applications. DirectFET is a trademark of International Rectifier.

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- 85% power loss reduction vs. diode ORing
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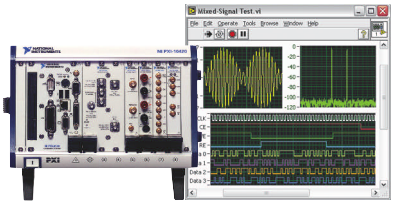

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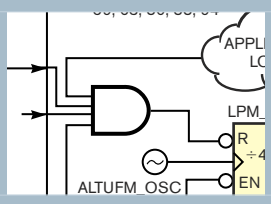

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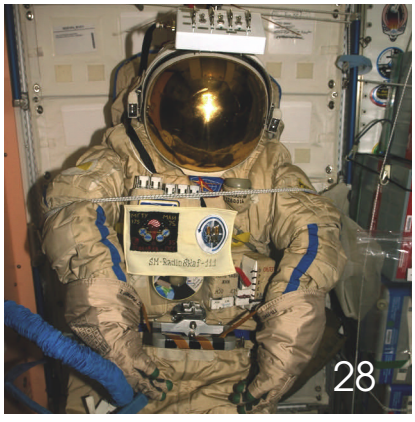

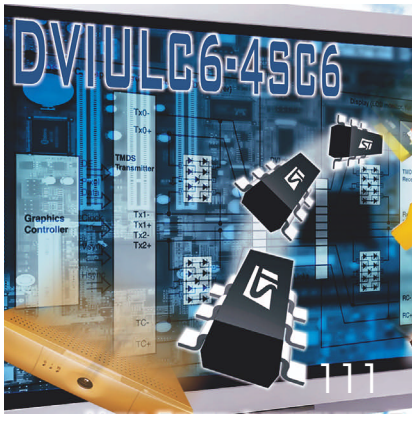

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Vol. IV, Issue 4

DESIGN | idea

Auxiliary Power Extends PoE Applications

by Joseph DeNicholas, Principal Circuit Design Engineer

Power-over-Ethernet (PoE) has found utility in hundreds of applications from Voice over Internet Protocol (VoIP) telephony and wireless routers to security equipment. Many PoE applications employ auxiliary power sources, typically an AC "wall wart" power supply at the Powered Device (PD) or an Uninterruptible Power Supply (UPS) at the Power Sourcing Equipment (PSE). Integrating auxiliary power can be a challenging design task and the PoE designer must understand the various methods and inherent tradeoffs that exist with each.

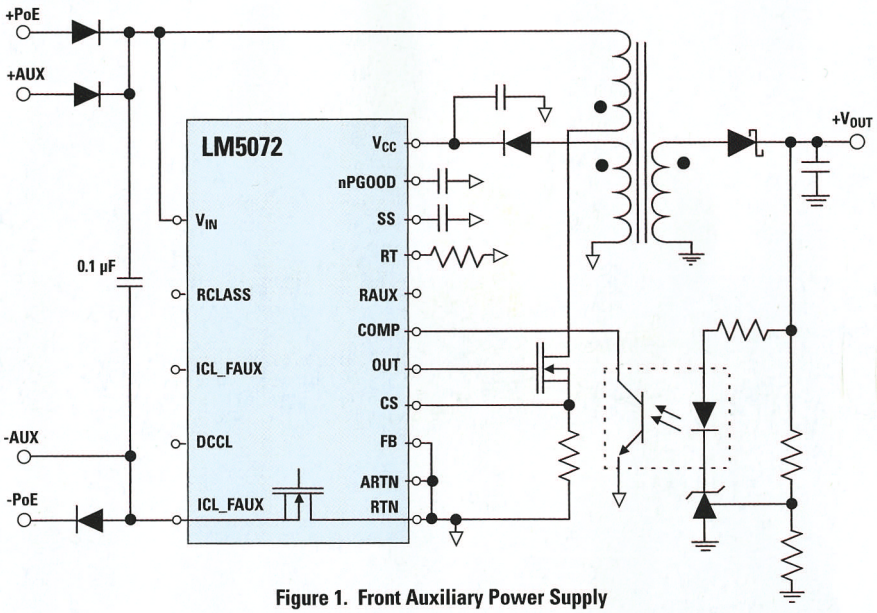

Figure 1. Front Auxiliary Power Supply

Three configurations are commonly used to add auxiliary power to PoE systems, and the possible combinations are to multiplex auxiliary power with PoE power (1) through the PD's front end hot-swap section, (2) directly to the input of the PD power supply controller, and (3) directly to the PD power supply's isolated output voltage.

In the first case, power is multiplexed into the PD's front end and delivered through the hot swap section. This is sometimes referred to as "front aux", and is illustrated in *Figure 1.*

Front aux has the advantage of hot swap protection, as power is delivered through the PD's PoE interface controller. If the front aux potential is lower than normal PoE levels, the first power source applied will deliver power indefinitely. This occurs because insertion of aux before PoE eliminates the ability of the PSE to detect the PD signature resistance; this will be the case whenever front aux is implemented. However, if PoE is supplied first, the lower potential aux supply will be blocked by the reverse biased aux power diode. One additional drawback to low voltage front aux is the potential for power draw limiting. This can occur when the hot swap current limit function restricts the current drawn from the aux supply.

If the front aux potential is comparable or higher than PoE, it further complicates the situation as the two supplies may share the PD load proportional to their regulation voltages and inversely proportional to their output impedances. Another serious complication exists when a higher

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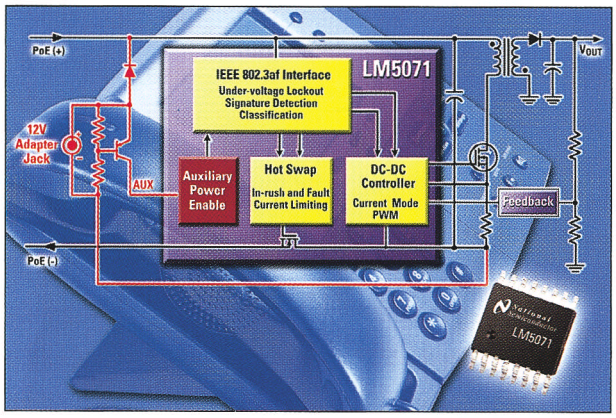
Featured Products

Power-over-Ethernet PD Controller With Auxiliary Power Interface

The LM5071 power interface port and Pulse Width Modulation (PWM) controller provides a complete integrated solution for Powered Devices (PD) that connect into Power-over-Ethernet (PoE) systems. The LM5071 is specifically designed for the PD that must accept power from auxiliary sources such as AC adapters. The auxiliary power interface of the LM5071 activates the PWM controller when the AC adapter is connected to power the PD when PoE network power is unavailable. The LM5071 integrates an 80V, 400 mA line connection switch and associated control for a fully IEEE 802.3af compliant interface with a full featured current mode pulse width modulator DC-DC converter. All power sequencing requirements between the controller interface and Switch Mode Power Supply (SMPS) are integrated into the IC.

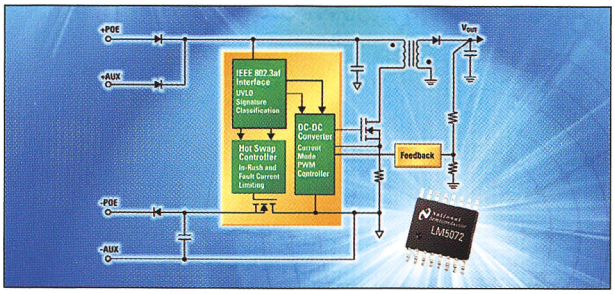


Features

- Compatible with 12V AC adapters
- Fully Compliant 802.3af power interface port
- 80V, 1Ω, 400 mA internal MOSFET
- Detection resistor disconnect function
- Programmable classification current
- Current mode pulse width modulator
- Supports both isolated and non-isolated applications

The LM5071 is ideal for use in devices powered by a PoE network including VoIP phones, security cameras, and wireless local area network (WLAN) nodes connected through Ethernet networking cables and ports. This device is housed in a tiny TSSOP-16 package.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LM5071.html



Single-Chip Power-over-Ethernet Device for Higher-Power PoE Applications

The LM5072 Powered Device (PD) interface and Pulse-Width-Modulation (PWM) controller provides a complete power solution, fully compliant to IEEE 802.3af, for the PD connecting into the Power-over-Ethernet (PoE) system. This controller integrates all functions necessary to simplify the implementation of both the PD power interface and the DC-DC converter with a minimum number of external components. The device includes an easy-to-use PWM controller that facilitates the implementation of single-ended power supply topologies including the flyback, forward, and buck. The LM5072 provides design flexibility by allowing the PD to also accept power from auxiliary sources such as AC adapters and solar panels, in a variety of configurations. The low R_{DSON} PD interface hot swap MOSFET and programmable DC current limit extend the range of LM5072 applications up to twice the power level of 802.3af compliant PD devices.

Features

- Fully compliant IEEE 802.3af PD power interface
- Versatile auxiliary power options
- 9V Minimum auxiliary power operating range
- 100V Maximum input voltage rating
- Programmable DC current limit
- Integrated PoE input UVLO and detection resistor
- Current mode PWM controller
- 100V Start-up regulator
- Supports isolated and non-isolated applications

Applications for the LM5072 include VoIP phones, remote security cameras, card readers, wireless access points, computer telephony, powered devices in PoE systems, and 48V telecom power supply controls. It is available in an exposed pad TSSOP-16 package.

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Auxiliary Power Extends PoE Applications

potential aux source is applied because it presents a new hot swap condition to the controller. The sudden increase in the input voltage of the PD controller may force the hot swap transistor into current limit as the MOSFET charges the input capacitor of the power supply. This will momentarily negate the system's input "Power Good" status which must be filtered in order to maintain continuous power delivery. The hot-swap controller should have its current limit set well in excess of the DC current being delivered to the load. If the DC current limit is set too low, there will be insufficient surplus current in the hot-swap controller to charge the load capacitors before an error occurs.

Power disconnection must also be carefully considered. If PoE power is not present, which is the case if front aux power was applied first, power delivery will not be maintained when aux power is removed because the module capacitors must completely discharge before the PSE will be able to detect a valid signature and reapply power. Continuity of power is guaranteed if front aux is present and PoE power is removed at any time.

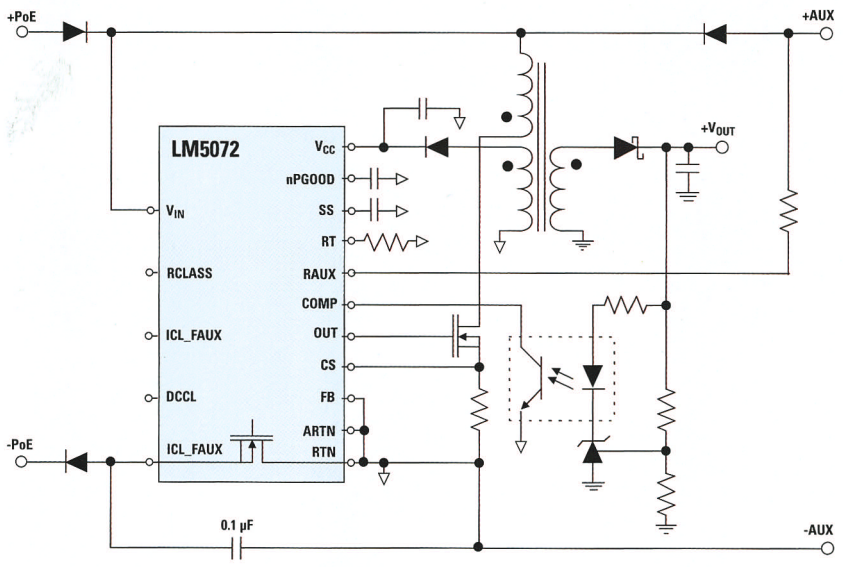

Figure 2. Rear Auxiliary Power Supply

Application of front aux power can be a difficult and confusing proposition. Many of the complications are alleviated if auxiliary power is supplied directly to the power supply section of the module (sometimes referred to as rear aux), as shown in *Figure 2.*

Rear aux will also be dominant if it is applied to the module first as it reverse biases the input diode bridges preventing the PSE from detecting a valid signature. Depending on the PD controller IC selected, the user may have the option of disabling the PoE interface upon application of the rear aux supply. When PoE power is disabled while aux power is available, the configuration is referred to as "aux dominant". The aux-dominant mode disables the hot-swap controller's power MOSFET switch, thereby preventing PoE power delivery. If DC Maintain Power Signature detection is performed by the PSE, as outlined in the IEEE 802.3 standard, the PSE will remove PoE power as it will consider the PD to be disconnected. This is a major advantage of the rear aux method because it offloads the PSE supply thus allowing power to be reallocated to other ports.

If the rear aux method is configured for non-dominance and PoE power is applied first, then the aux supply will not deliver power until PoE power is removed. Just as in the front aux case, power delivery to the load will be maintained in dominant or non-dominant mode so long as the rear aux supply is present. If aux power is removed and PoE power is not enabled (because of aux dominance or aux being applied first), continuity of power delivery will not be maintained.

The final option, where auxiliary power is OR'd directly to the output of the PD power supply, is a simple solution but offers few advantages. It requires an aux power supply that is designed to deliver the current and regulated voltages required by the PD load. In addition, this configuration usually requires additional components and some duplication of functions, possibly even a second isolated switching regulator or a linear post regulator.

The addition of auxiliary power to PoE-powered devices can be a complex and daunting task. Only by understanding the costs, benefits, and constraints of each configuration can the designer of PoE-enabled equipment select the appropriate scheme and deliver the desired system performance. ■

For more information on power supply design for PoE applications, read Power Designer #104 at power.national.com/designer

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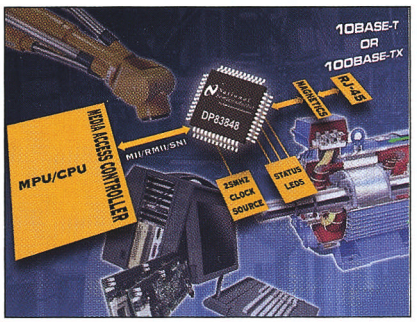
DP83848 PHYTER 10/100 Single-Port Physical Layer Device

The PHYTER® family of transceivers addresses the quality, reliability and cost requirements of embedded developers networking their devices for the home, industrial, and environments requiring an extreme temperature range. In addition to key features such as IEEE 802.3u specification compliance, UNH interoperability certification, Auto-MDIX up to 150 meters of cable reach, and superior ESD protection (4.0 kV) National's DP83848 incorporates a number of system cost-reducing features not found on other suppliers' physical layer products (PHYs). For example, the DP83848 incorporates a 25 MHz clock-out that eliminates the need, and hence space and cost, of an additional media access control (MAC) clock source component.



Features

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  – *Guaranteed by Test*
- UNH compliant
- Lowest latency for real-time operation
- Integrity utility for system monitoring and maintenance
- 4 kV ESD protection (HBM)
- 25 MHz clock output
- Low power <270 mW
- Auto-MDIX
- Selectable MII/RMII interface

The DP83848 PHYTER is offered in tiny LQFP-48 packaging, and is ideal for embedded computers, high-end peripherals, industrial controls, building/factory automation, transportation, test equipment, and wireless basestations.

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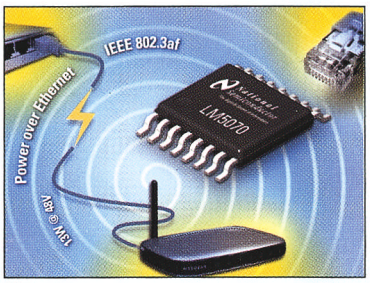
Integrated Power-over-Ethernet PD Interface and PWM Controller



The LM5070 power interface port and Pulse Width Modulation (PWM) controller provides a complete integrated solution for Powered Devices (PD) that connect into Power-over-Ethernet (PoE) systems. The LM5070 integrates an 80V, 400 mA line connection switch and associated control for a fully IEEE 802.3af compliant interface with a full featured current mode pulse width modulator DC-DC converter. All power sequencing requirements between the controller interface and Switch Mode Power Supply (SMPS) are integrated into the IC. Two options are available providing either an 80% maximum duty cycle limit with slope compensation (on the –80 suffix) device or a 50% maximum duty cycle limit and no slope compensation on the (–50 suffix) device.

Features

- Fully-compliant 802.3af power interface port
- 80V, 1Ω, 400 mA internal MOSFET
- Programmable inrush current limit
- Detection resistor disconnect function
- Programmable classification current
- Programmable under-voltage lockout with programmable hysteresis
- Thermal shutdown protection
- Current mode pulse width modulator
- Supports both isolated and non-isolated applications
- Error amplifier and reference for non-isolated applications

The LM5070 is available in TSSOP-16 and LLP-16 packaging and is ideal for use in PoE network-powered devices such as IP phones, security cameras, Wireless Local Area Network (WLAN) nodes and even musical instruments through Ethernet networking cables and ports.

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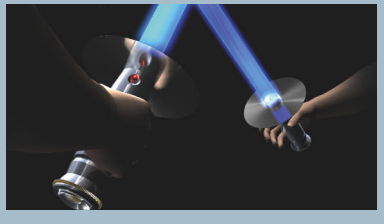

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EASING THE MODELING OF LOSSY LINES (pg 79):

What you lose from a lossy line
→ www.edn.com/article/CA379881

Modeling gigabit backplanes from measurements
→ www.edn.com/article/CA509596

Signal-integrity modeling of gigabit backplanes, cables, and connectors using TDR
→ www.edn.com/article/CA231568

BY MAURY WRIGHT, EDITOR IN CHIEF

Serving you: the *EDN* mission

I recently read several hundred comments from *EDN* readers that we gathered as part of one of our numerous research projects. The comments convinced me that I should share some things about how and why we do things at *EDN* and highlight some resources that some of you may be unaware of. I'm focusing on making *EDN* your most trusted source for technical information. I believe that serving the reader is the foundation upon which to build successful information sources and our publisher, John Schirmer, mandates *EDN*'s focus on this mission.

We take research seriously because it helps us improve our print magazine, Web site, newsletters, and other offerings. We do an annual research project in which we ask you to measure us against the competition. We do special projects, such as a study we did with the launch of our redesign last summer. We do monthly research on issue content. And, every two years, we do a major "Mind of the Engineer" study. Thanks to all that take time to participate; your input is invaluable.

The comments I recently read varied from specific advice to general praise, such as "good job." One reader suggested about the print magazine, "Send it with a cold six-pack and $20 for take-out pizza." Something tells me my boss won't approve of that approach.

Several of you expressed dislike for our practice of running article sidebars or other information, such as tables or figures, only on the Web. At least a couple of you explicitly stressed that we should stop trying to drive you to our Web site. I'd like to share my conundrum. I'll admit that we would like you all to visit our site. We do sell advertising on the site, but I also believe that we offer value to visitors. In fact, the Web allows us to present information that we once would have lost on the cutting-room floor. Our print business model has always limited the pages for each issue and article. Before the existence of our Web site, we were sometimes unable to present valuable information that didn't fit into print. I hope most of you agree that it's better for us to offer such information on the Web as a complement to the print articles.

The Web allows us to present information that we once would have lost on the cutting-room floor.

Many of you dislike advertising mixed in with articles and especially the ads on heavier page stock. I'm sorry about those disappointments, but those things pay the freight, and there is simply nothing we can do if we want to provide you with the maximum number of print editorial pages.

I know many of you specialize in analog-circuit design and embedded software, for example, and a number of other disciplines, because you asked for more coverage in those areas. *EDN* is a horizontal-market book for the design engineer. We strive to offer a balance of information in each issue across disciplines, products, and end applications.

Many of you asked for more Design Ideas. Frankly, we run most of the good ones that we get. Overwhelm us with more, and we'll see about more print pages or perhaps present some in newsletters or on the Web site. We also have a section, "Tales from the Cube," that we launched last June. Research says that you like that better than any of the other new departments. Please support the section by submitting your own first-person "tale" and collecting $200.

A number of you also asked for more back-to-basics tutorials. We've had the same thought. We are looking at ways to offer such primers—in print or on the Web. We already offer what quite a few readers asked for: free archives on the Web going back more than 10 years. Also, you can still get a PDF of archived articles. We've changed the Web button from "PDF" to "printer-friendly version," but we didn't remove the PDFs.

I'll close by also thanking all of you who voted in our annual Innovation Awards program. I know participating takes time, but you are part of choosing the most innovative technologies each year. You will find the winners in the article starting on pg 33 of this issue.EDN

Call me at 1-858-748-6785 or e-mail me at mgwright@edn.com.

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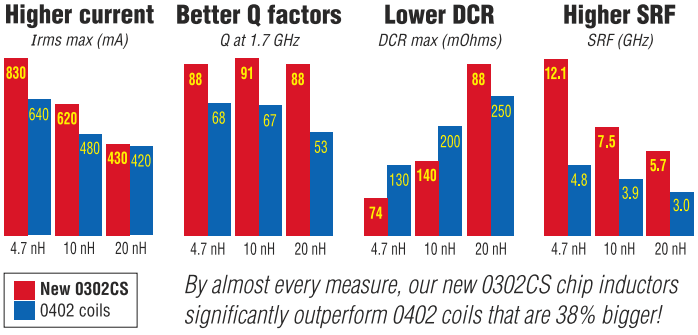

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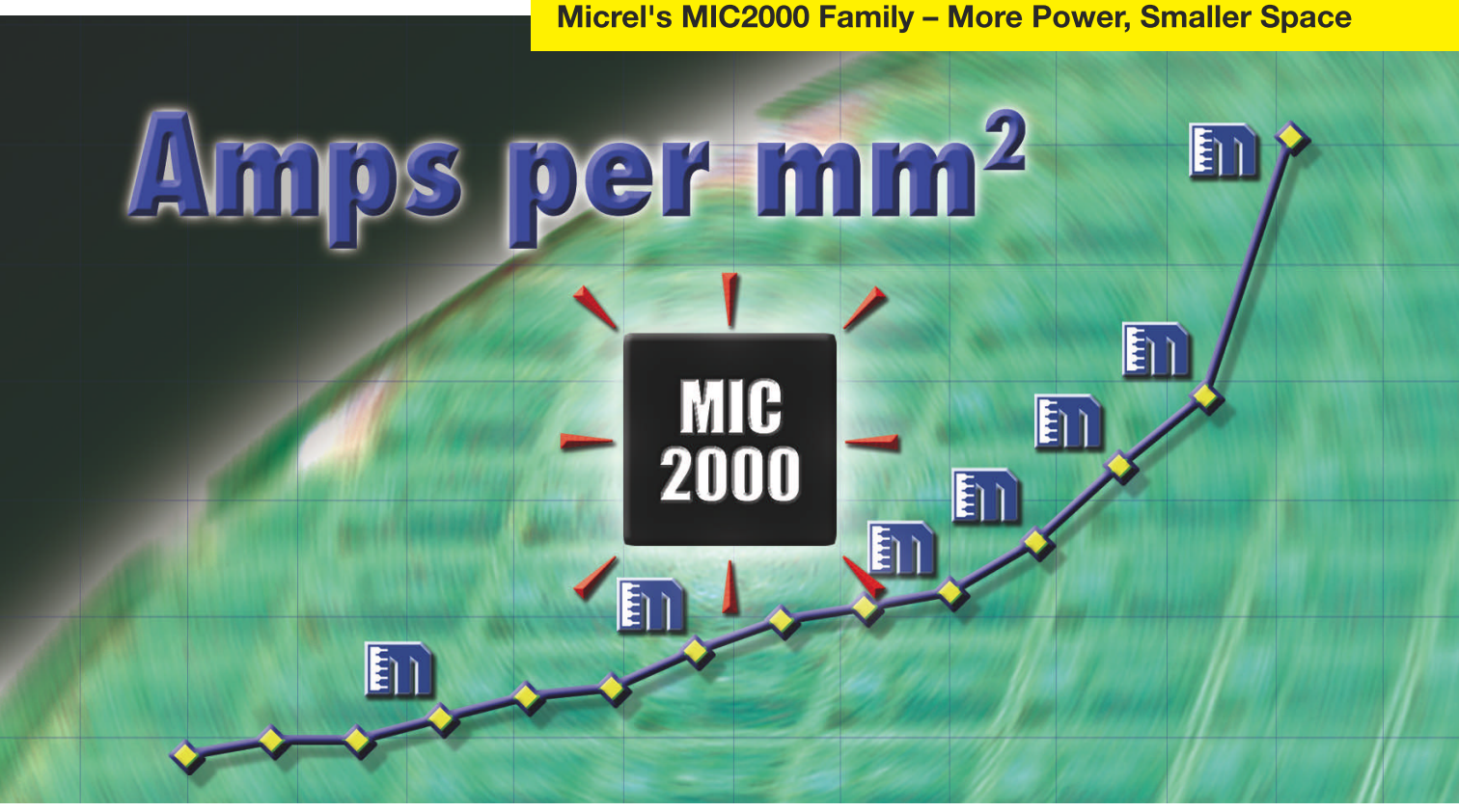

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2005	2015		~	◆	◆	◆	~	~
2006	2016		~	◆	◆	~	◆	~
2007	2017	ADJ	◆	◆	◆	~	~	◆
2008	2018		◆	◆	◆	~	~	~
2009	2019		◆	◆	~	◆	~	~

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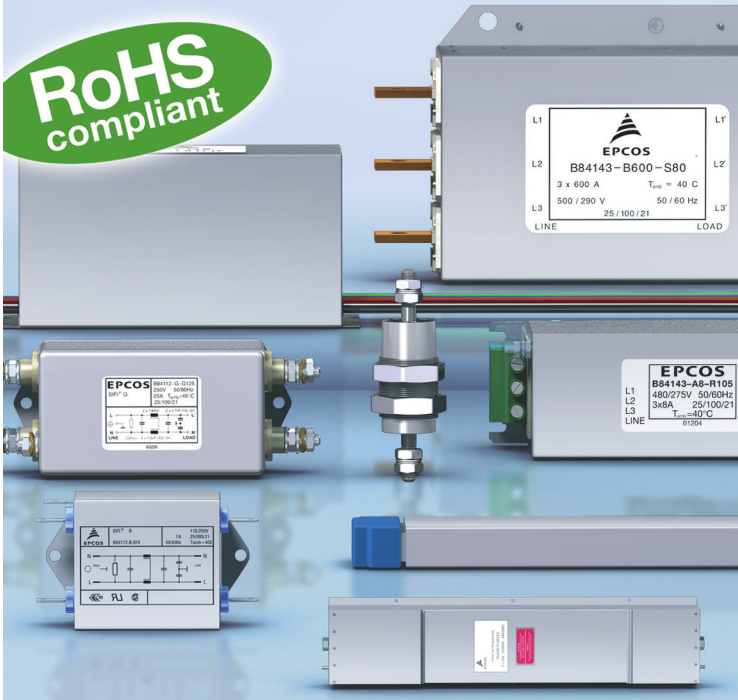

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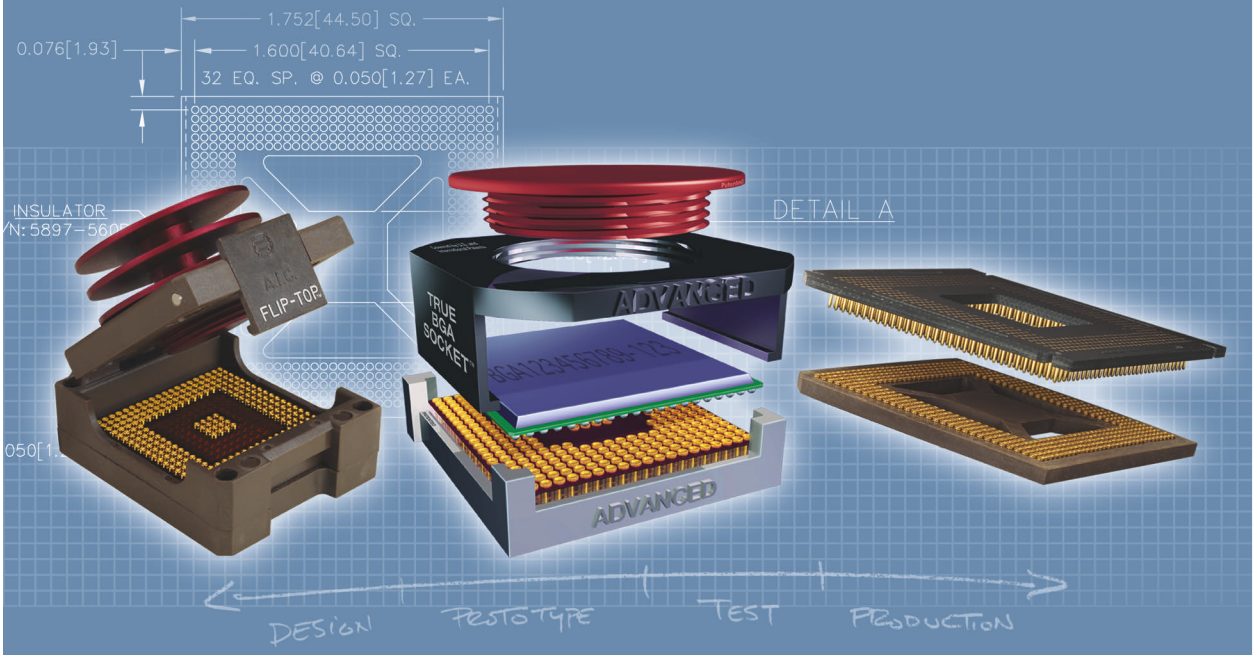

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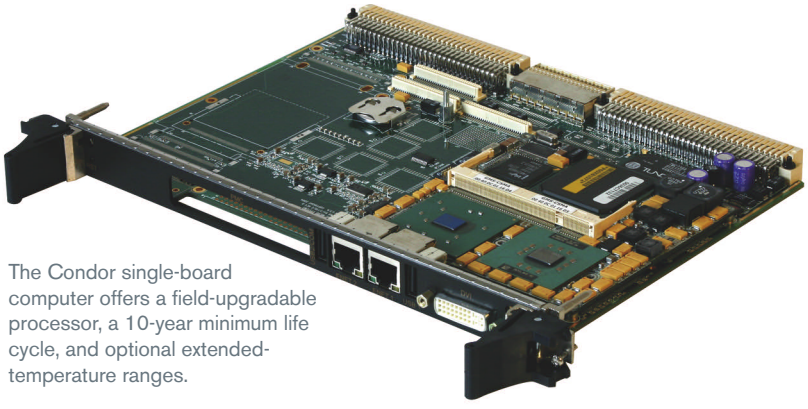
INNOVATIONS & INNOVATORS

CPU module extends product life span

With a mezzanine concept that updates the CPU instead of the I/O, General Micro Systems claims that its latest VMEbus-based single-board computer virtually eliminates processor obsolescence. The V265 Condor's 4×4-in. processor module enables field upgrading of the processor to meet performance and technological requirements over the typical 10-year life cycle of embedded systems. The current Pentium M processor enables an array of options ranging from the low-power, low-cost Celeron M 373 to the high-performance, 1.8-GHz M-745.

Condor provides as much as 2 Gbytes of 266-MHz DDR SDRAM. With multiple serial- and parallel-I/O choices, it supports as many as 10 multiprotocol-communications controllers. To satisfy rear-I/O requirements, customers may also select which onboard I/O options to channel through the VME P2 and P0 connectors. The onboard dual-pipe video controller with 64 Mbytes of 64-bit memory provides two independent video channels, each with 2- and 3-D accelerations and resolution of 2048×1536 pixels at 75 Hz with 24-bit color.



The Condor single-board computer offers a field-upgradable processor, a 10-year minimum life cycle, and optional extended-temperature ranges.

The V265 Condor board is available in both convection- and conduction-cooled versions. The board supports Windows, VxWorks, and Linux operating systems. Prices start at $2156 (100).

—by Warren Webb

▶**General Micro Systems**, www.gms4sbc.com.

High-end and economy FPGAs target communications

Apparently unafraid of going toe to toe with Xilinx (www.xilinx.com) and Altera (www.altera.com) in the high-end-SRAM-based-FPGA market, Lattice Semiconductor has announced a high-performance FPGA targeting the high-speed-communications and data-storage-design markets. The company is also releasing an "economy-class" FPGA. Both new device families consume less power and have greater density than previous Lattice offerings, thanks to fab partner Fujitsu's (www.fujitsu.com) 90-nm process, according to Stan Kopec, Lattice's corporate vice president of marketing. The company implemented the previous generation in a 130-nm process. On top of the inherent improvements from the process reduction, Lattice has also added several new features to its LatticeSC and LatticeECP2 offerings.

Lattice has added a high-channel-count SERDES (serializer/deserializer) supporting 3.4-Gbps data rates, 2-Gbps Pure-speed parallel I/O, and new clock-management structures that allow the FPGAs' logic to operate as fast as 500 MHz. One family member also includes precoded structured-ASIC blocks. The LatticeSC family offers four to 32 SERDES channels. The family will include five products, ranging in density from 15,200 look-up tables or 152,000 ASIC gates in the SC15 to 115,000 look-up tables or 1.15 million ASIC gates in the SC115. You can reconfigure the look-up tables as SRAM for the device, which includes as much as 7.8 Mbits of embedded SRAM. The devices operate from a 1 or 1.2V supply. To help users manage setup-and-hold-time margins at input registers, each LatticeSC I/O pin includes an input-delay alignment block with 144 taps at 40-psec intervals.

Lattice will also offer the SC-M variation of the SC device, which adds preconfigured, structured-ASIC blocks to the FPGA. The structured-ASIC blocks, which are the unused areas of the SC device, add 50,000 ASIC gates to the standard SC architecture. The structured blocks add 1- and 10-Gbps Ethernet; PCIe (PCI Express); DDR1/2, QDR2, and RLDRAM controllers; and SPI4.2.**—by Michael Santarini**

▶**Lattice Semiconductor**, www.latticesemi.com.

MEMS-based oscillator threatens quartz; resonator could move on-chip

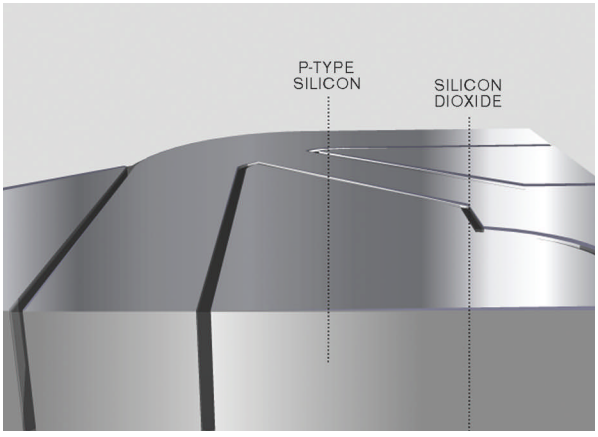
Few electronic components have stood the test of time better than the quartz-crystal oscillator or resonator. But researchers continue to search for a quartz replacement because the components don't scale downward sizewise—at least relative to ICs—and manufacturing and packaging are problematic, even though the industry has developed ways to turn out millions of discrete oscillators at low prices. MEMS (microelectromechanical-system) technology is one silicon technique that designers can use to build an oscillator. Start-up SiTime believes that it has unlocked the secret to MEMS-based oscillators that, as discrete components, can undercut quartz prices and that designers might ultimately integrate directly into large digital chips.

SiTime claims that vendors this year will manufacture 10 billion quartz crystals with complex popular products, such as handsets, hosting a half-dozen or more such components. Despite challenges from ceramic and silicon approaches, quartz has remained dominant due to excellent temperature-stability and phase-noise performance. Early silicon-based MEMS oscillators failed to offer such stability due to both the temperature properties of silicon and contamination that gathered on the vibrating beams in MEMS oscillators.

SiTime claims to have solved the MEMS-oscillator problem with a packaging technology. The company has addressed problems associated with earlier MEMS-oscillator packages using the MEMs First silicon-process technology, which it based on SOI (silicon-on-insulator) wafers. In MEMS First, a silicon etch creates 10-micron trenches that form the resonator beam. The process then relies on glass that fills in the trenches, so that an epitaxial reactor can grow a layer of silicon and polysilicon on top. The process then relies on vents that are etched in the silicon so that hydrofluoric acid can remove the glass, freeing the beams to oscillate. The reactor again seals the cavities, leaving a clean vacuum underneath. SiTime claims that the process eliminates stability problems and offers better stability than quartz technology. Further, the semiconductor process can churn out oscillators that are a fraction of the size of quartz.

Initially, SiTime will package its resonators as direct replacements of quartz resonators, simply offering a lower price and presumably superior performance. Among the offerings is the SiT8002 programmable oscillator that can output a signal ranging from 1 to 125 MHz. The product will sell for 69 cents (1 million). Meanwhile, the SiT11xx family of fixed-frequency oscillators will sell for 49 cents (1 million). The company may later use the MEMS First process to embed oscillators in the substrate below CMOS digital ICs.**—by Maury Wright**

▷**SiTime**, www.sitime.com.



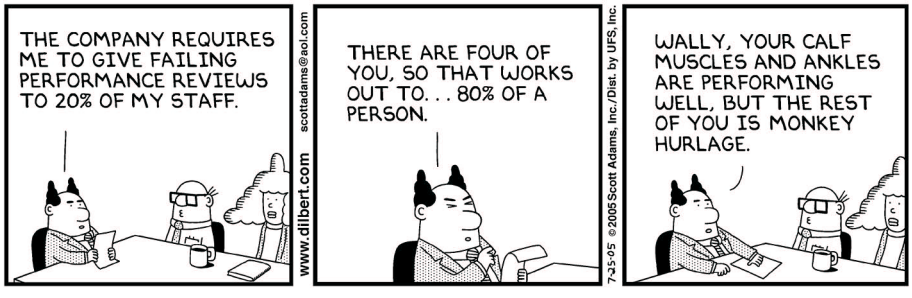
Trenches etched in a silicon substrate form MEMS beams that oscillate in SiTime's MEMS-based-resonator product line.

FROM THE VAULT

Electronics occupies a unique engineering niche. Next year's jets won't fly twice as high or use half as much fuel, and, except for the pinstriping, next year's cars won't differ markedly from this year's ... Today, just 40 years after the invention of the transistor and 15 years after the appearance of the first 4- and 8-bit microprocessors, manufacturers have found a commercially practical way to put 1 million transistors on a single chip. Some industry experts predict that, by the year 2000, engineers will be working with billion-transistor chips, which represent a thousandfold increase over today's device density.

Steven H Leibson, Regional Editor, *EDN*, March 3, 1998.

DILBERT *By Scott Adams*



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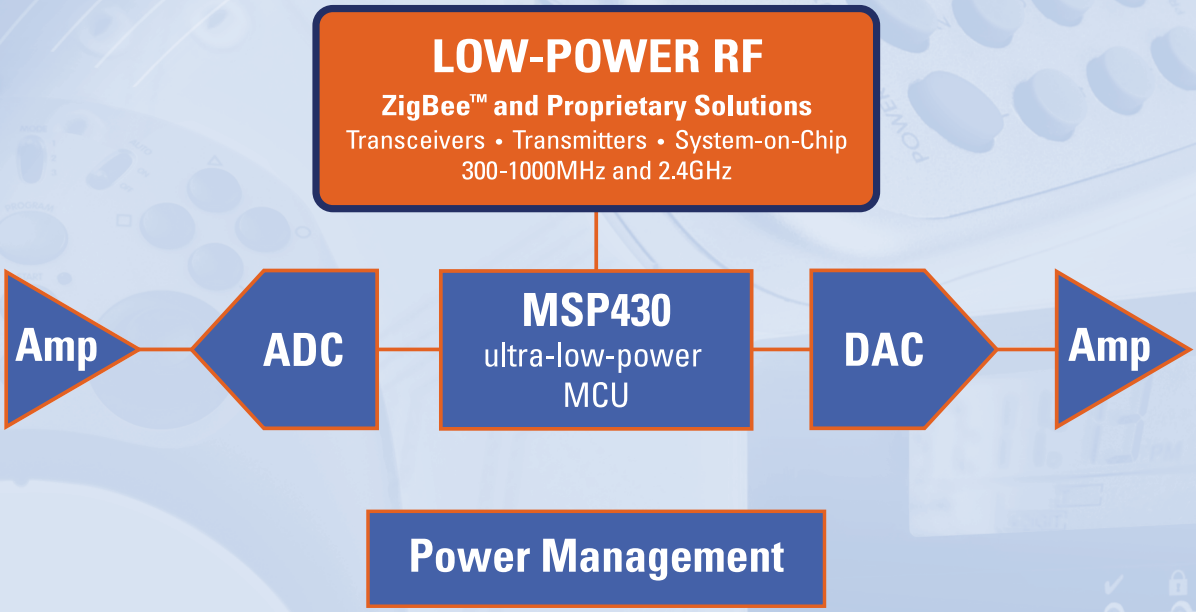

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Device combines signal and power isolation

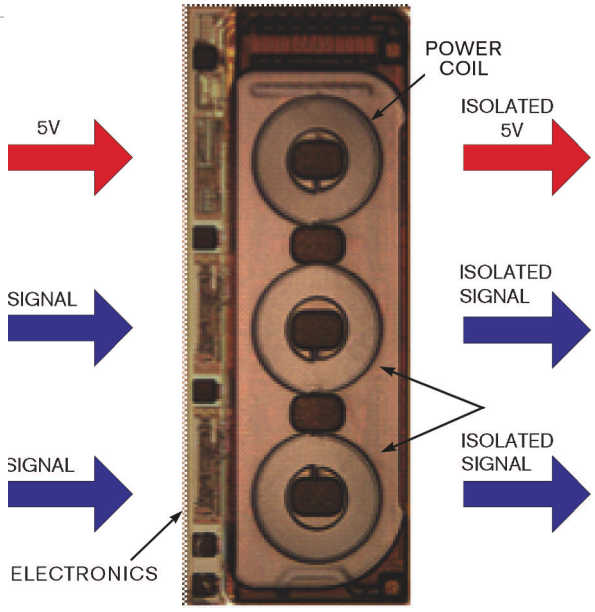
Building on its iCoupler technology, which includes chip-scale microtransformers directly in the chip substrate, Analog Devices is offering what it claims is the first device to combine signal and power isolation in the same chip. The ADuM524X isoPower family of dual-channel isolators integrates isolated power supplies and regulators that provide as much as 50 mW of isolated, regulated power at 5V with two isolated digital-signal channels. The devices target low-power isolation, such as that in factory-automation equipment, instrumentation, and secondary-control power supplies.

One popular method of signal isolation uses optocouplers, which combine LEDs and photosensitive transistors, but these devices have limitations: Their characteristics can vary with age and temperature. In addition, although optoisolators can isolate signals, they can't isolate power. The isoPower technology, which Analog Devices based on planar transformers, can do both signal and power isolation in one package for a significant cost and space savings and still provide isolation ratings as high as 5 kV.

The ADuM524X family members vary by the directionality of each channel. The ADuM5240, targeting data-acquisition applications, has two signal outputs on the same side as the power output. The ADuM5241 has signal channels in each direction, and it targets bidirectional communications, such as RS-232 transceivers, that require isolated power for interface electronics. The ADuM5242, with the two signal outputs on the same side as the power input, targets power-supply applications that employ secondary-side control and require isolated power to initiate start-up. The devices come in eight-lead, narrow-body, lead-free SOIC packages and cost $2.95 (1000).

—by Margery Conner

▷**Analog Devices**, www.analog.com.



ADuM524X products incorporate the isoPower technology, which integrates an isolated dc/dc converter with two channels of digital-signal isolation in an eight-lead SOIC.

FEEDBACK LOOP

"Datapath issues may be the biggest challenge facing chip designers today and in the future. Validation and lithography simulation simply take too much time on current platforms."

Jim McKibben in *EDN*'s Feedback Loop at www.edn.com/article/CA6297764. Add your comments.

RFID and 802 marriage targets asset-tracking systems

Most RFID target applications to date have relied on relatively short-range links between the ID tag and the reader. Officials at start-up G2 Microsystems believe that the short-range approach is wrong for many applications. The company claims that designers place too much emphasis on low-cost RFID tags and not enough on the cost of the wireless infrastructure that connects to the tags. Without question, retail-inventory applications require cheap tags. But G2 officials believe that applications such as tracking medical instruments within a hospital or pallet arrivals in a warehouse need the already-deployed and paid for Wi-Fi networks in facilities ranging from factories to hospitals. So, G2 developed the G2C501 SOC (system on chip), which combines a 32-bit CPU, an 802.11b client interface, and support for a variety of RFID-tag technologies.

Of course, power consumption is a key challenge for an 802.11-based RFID tag. Mainstream Wi-Fi technology proves to be a battery drain on notebook PCs, and an RFID tag needs to live for perhaps years on a small battery. Indeed, power concerns led the G2 team to integrate a proprietary 802.11b design rather than use a low-cost, off-the-shelf chip. The company claims to have re-examined how 802.11b works and how to reduce power in a client that infrequently transmits only short bursts of data. G2 claims that a tag based on its chip can last five years, reporting every 40 seconds, using two AA batteries. The IC also supports location reporting to within 3m based on the ISO 24730 standard. Samples are available now, and the chip will sell for $12 (high volumes). A full evaluation kit with software-development tools sells for $1500.

—by Maury Wright

▶**G2 Microsystems**, www.g2microsystems.com.

04.13.06

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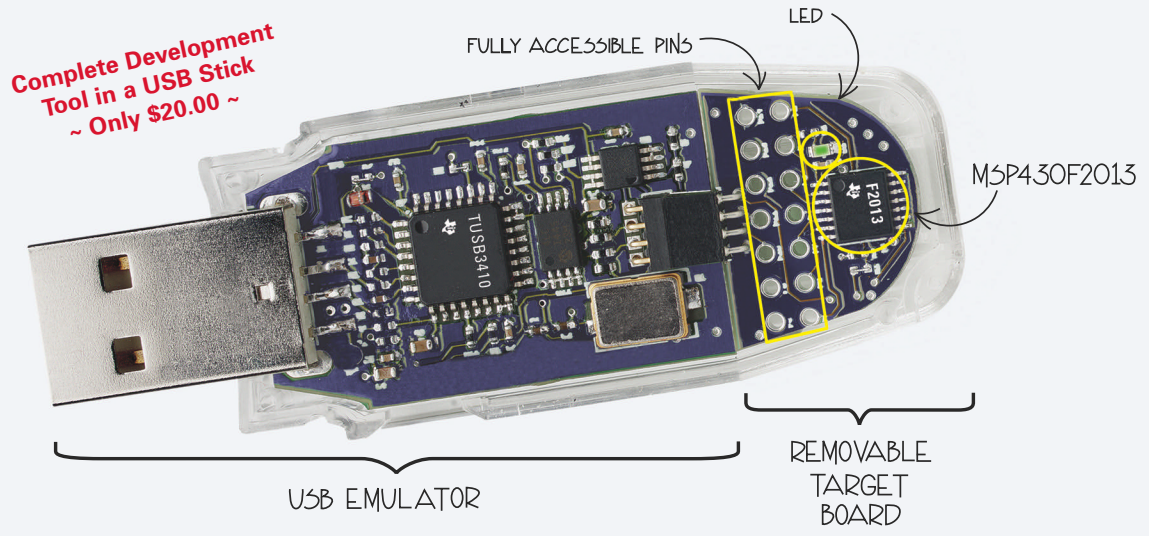

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MSP430F2012	2 KB	128 B	✓	10-bit ADC	$1.15
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VOICES

August Capital's Andy Rappaport on innovation

An engineer turned entrepreneur and then venture capitalist, Andy Rappaport also did a stint as a senior editor for *EDN,* following ASIC technology in the early '80s. Rappaport's career has mandated that he be a keen judge of innovation, so, naturally, he was a perfect choice as featured speaker at *EDN*'s annual Innovation Awards banquet on April 3 in San Jose, CA. Before the talk, Rappaport shared some of his experiences. For an expanded version of this interview, go to www.edn.com/060413p1.

How do you define innovation? Is it restricted to completely new ideas? Can it be realized in simply engineering a better way to handle a known task?

A I make a distinction between invention and innovation. Inventions are new ways of doing things and can take many forms. Sometimes, they lead to successful products or companies. But innovation is something that alters the world in a fundamental way. The Wallace Tree multiplier was a neat invention, but the programmable DSP turned out to be truly innovative.

What true innovations industrywide have you most admired over your career, and feel free to go back as far as you like, because this is our 50th anniversary publishing *EDN*, and we're looking back, as well.

A It's hard to think of anything in the electronics sphere more important than the planar IC. Nobody remotely understood how important small was when [Robert] Noyce and [Jack] Kilby got the ball rolling on integration. The microprocessor and programmable DSP are two related innovations that have clearly changed the world during my career. CMOS is another. By simplifying the interface between process and circuit design, it democratized access to IC technology in ways it was hard to imagine as it was happening. TCP/IP ranks up there, too. I love that it has exceeded the bounds that even [Ethernet inventor] Bob Metcalf thought would kill it. The greatest innovations always surprise their progenitors that way.

As an investor and entrepreneur, what are the applications that you have been involved in that have excited you the most?

A I was involved in the birth of the FPGA 20 years ago. That was exciting, especially because virtually everybody not involved in FPGAs at that time thought the whole notion was crazy. I have also been involved in driving the use of unlicensed spectrum for serious communication for more than 15 years. I've been able to take part in the recent explosion of Wi-Fi, and I am looking forward to seeing technologies such as this capture voice and media traffic. I believe that most of the economic value of radio communications will switch from licensed to unlicensed spectrum over the next 20 years, and shifting economic value is how venture capitalists succeed.

I have also been gratified to have been involved early in the whole fabless-semiconductor revolution. People forget now how controversial the notion was 20 years ago. But the ability to make state-of-the-art process technology available to designers unable to invest in fabs has increased innovation by orders of magnitude relative to what it would have been otherwise. I was unpopular for a while in Silicon Valley for advocating this notion as strongly as I did early on. But the result has made it worth it.

At a pure R&D or laboratory level, what are the future enabling technologies that excite you the most and why?

A I am involved now with a company that is integrating optical and electronic devices at subwavelength scale. I am not nearly smart enough to predict which uses of this technology will ultimately prove most important, but the potential is vast, because it is becoming highly inefficient to use copper to communicate high-speed data. I am also betting that memory technology will change based on material science, not device design alone, because we are both reaching the density and performance limits of technologies deployed now and rapidly gaining understanding of how to use newly discovered effects.

I am also watching technologies that improve energy-storage densities. Electronic devices are on a trajectory to smaller size and greater portability. Delivering more energy in smaller packages is critical to allowing this trend to continue.

When you were at *EDN*, the ASIC industry was in its infancy, and you made some early predictions about how many ASIC designs would ultimately get done. Does it surprise or disappoint you that ASIC starts are now falling?

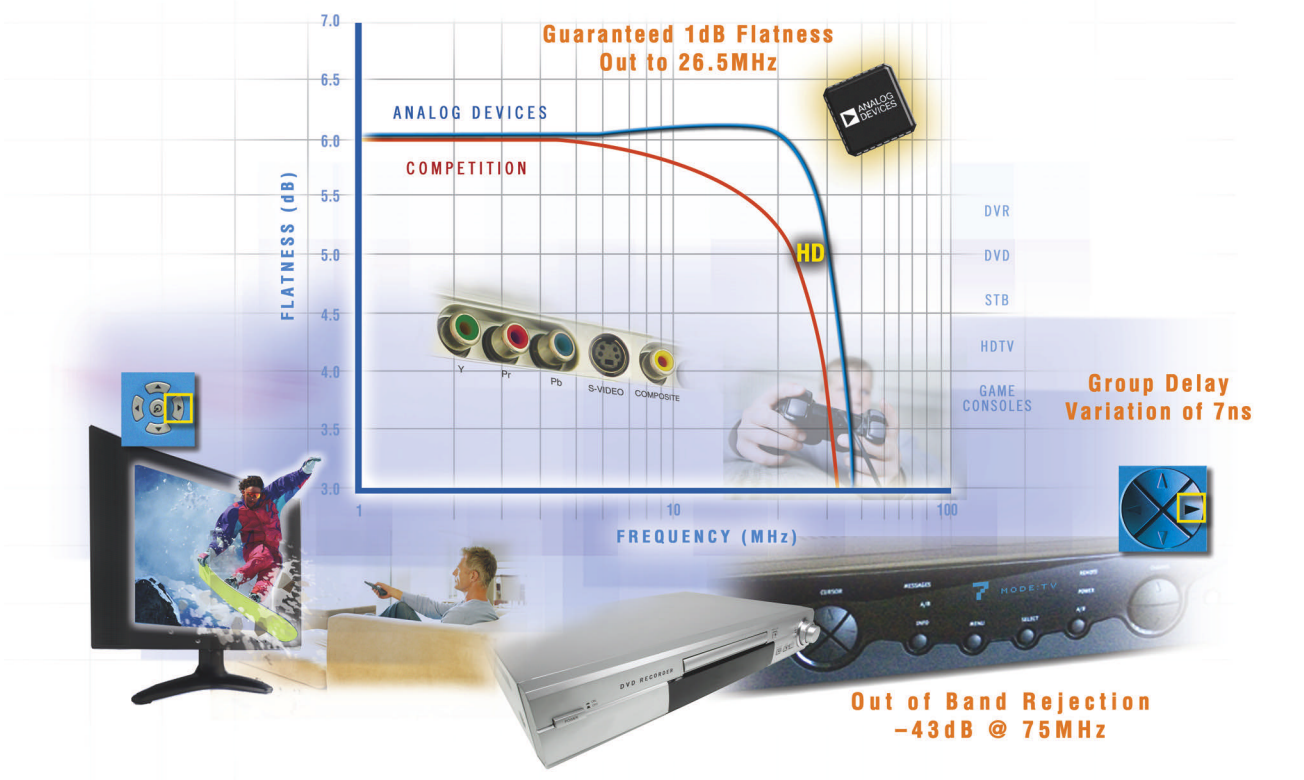
A ASIC is a methodology, and, like all methodologies, its effectiveness is a function of the technology and design intent to which you apply it. ASICs were all about making integration of custom logic economical. But technology has changed in two important ways.

First, logic inefficiency is no longer expensive. Current levels of integration make it unnecessary to optimize logic for most applications. You can define relatively general-purpose, software-programmable processors in a way that works well enough for most applications. The effort to further optimize transistor efficiency in most cases is not justified. So, a few basic architectures with little custom logic can satisfy most new designs. And IC processes have become complex to the point at which bearing the cost of design verification and masks is unwise unless it yields enormous benefit. So, we will see a trend toward fewer and fewer processor-based architectures doing most of the work in most systems with whatever custom logic is needed implemented in relatively small FPGAs or emulated in software or firmware.

–by Maury Wright

Integrated video filters with HD performance, guaranteed.

In video signal paths, analog is everywhere.



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- Rail-to-rail output
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Part Number	Channels	SD	HD	Selectable Gain	DC Adjust	2:1 Mux	Price @ 100k ($U.S.)
ADA4410-6	6	Y	Y	Y	Y	Y	1.80
ADA4411-3	3	Y	Y	Y	Y	Y	1.49
ADA4412-3	3	Y	Y	N	Y	N	1.29

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Looking for integrated antialiasing, reconstruction video filters that deliver reliable HD quality video? Our new ADA441x family guarantees a minimum flatness response of 1 dB out to 26.5 MHz, out of band rejection of –43 dB @ 75 MHz, and 7 ns group delay variation to enable the highest quality HD video.

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Performance and value define video designs, and Analog Devices defines the possibilities with industry-leading ICs, including:

- ADA4430-1 low power, standard definition (SD) integrated video filter
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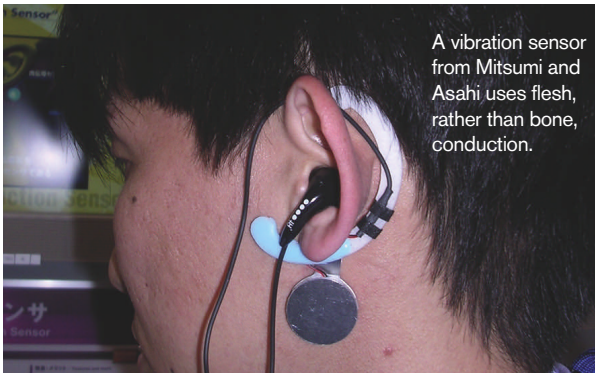

A vibration sensor from Mitsumi and Asahi uses flesh, rather than bone, conduction.

GLOBAL DESIGNER

Flesh-conduction microphone targets mobile phones

Mitsumi Electric Co and Asahi Kasei Corp have jointly developed a flesh-conduction vibration sensor with high sensitivity for voice input in mobile phones. Mitsumi demonstrated a microphone of mobile phones as an application at its private show, Mitsumi Show 2006. The sensor picks up vibration from vocal cords in a human body to operate as a microphone. At the demonstration of the vibration sensor, an operator placed the device under his ear and spoke into a mobile phone. A receiver picked up his voice, despite the noisy environment.

The vibration sensor uses flesh, rather than bone, conduction. A sensing portion attaches with soft silicone resin, which behaves the same as conduction in human skin. This approach avoids attenuating and reflecting the human voice. The microphone picks up voices over a 100-Hz to 3.5-kHz frequency range; it uses a 3V supply and a 500-μA current. The sensor integrates a sound-correction circuit with a capacitive sensor, measuring 20 mm in diameter and 5 mm thick.

—by Shoko Kawamura, Contributing Editor, *EDN Japan*

▷**Mitsumi Electric Co Ltd**, www.mitsumi.com.

▷**Asahi Kasei Corp**, www.asahi-kasei.co.jp.

Web sites offer verification help

At last month's Design Automation and Test Conference in Munich, Germany, Cadence released three Web sites to help customers create new verification methodologies or optimize established ones. Part of the company's Plan-to-Closure Web site, the new sites are Incisive Plan-to-Closure, Community Plan-to-Closure, and My Plan-to-Closure. Steve Glaser, vice president of marketing for Cadence's Verification Division, says that the sites will help users adapt advanced verification methodologies that often include a mix of languages, including SystemVerilog, VHDL, and SystemC.

The Incisive Plan-to-Closure gives customers access to Cadence resources for verification. It includes Web-based documentation for verification best practices, executable golden examples, technology libraries, templates, and access to deployment experts and Cadence's sales team.

The Community Plan-to-Closure allows Cadence users to share their verification methodologies, tips, and tricks with each other. It gives users access to frequently asked questions, registered Cadence universal-reuse-methodology prefixes, and paper presentations. Users can also download, upload, and share code and libraries. The site also includes forums addressing subjects such as verification planning and management, assertion-based verification, universal reuse, and system verification.

The customizable My Plan-to-Closure allows users to customize their Web sites to monitor, for example, code additions, forums, and updates pertaining to their jobs or projects.

—by Michael Santarini

▷**Cadence Design Automation**, www.cadence.com.

Dual-mode platform for mobile phone takes advantage of global expansion

04.13.06

Renesas Technology plans to develop the SH-Mobile G Series, an integrated platform with software and dual-mode application processors, for 3G mobile phones. The company expects to complete the joint project with NTT Docomo (www.nttdocomo.com), Fujitsu (www.fujitsu.com), Mitsubishi Electric (www.mitsubishi.com), and Sharp (www.sharp.com) by the second quarter of the 2007 fiscal year. Renesas expects the dual-mode platform to expand its SH-Mobile SOC (system-on-chip) business, including W-CDMA (wideband-code-division-multiple-access) technology from NTT Docomo and GSM/GPRS (Global System for Mobile communications/General Packet Radio Service) from European companies.

SH-Mobile G2 will support broader-band communication systems than its predecessor, SH-Mobile G1, and will also support HSDPA (high-speed-downlink-packet access) as fast as 3.6 Mbps and EDGE (Enhanced Data for GSM Evolution) at its baseband circuit. The G2 will become available for sampling in July 2006 to the OEMs of Fujitsu, Mitsubishi, and Sharp. The G2 chip will enter volume production in the second quarter of 2007.

The platform comprises SymbianOS as an operating system and an MOAP (mobile-phone-oriented application platform) from NTT Docomo. Renesas plans to later support Linux. The platform also comprises the SH-Mobile G2 hardware chip, device drivers, middleware, communication-control software, OS, and application software.

—by Takatsuna Mamoto, Editor in Chief, *EDN Japan*

▶**Renesas**, www.renesas.com.

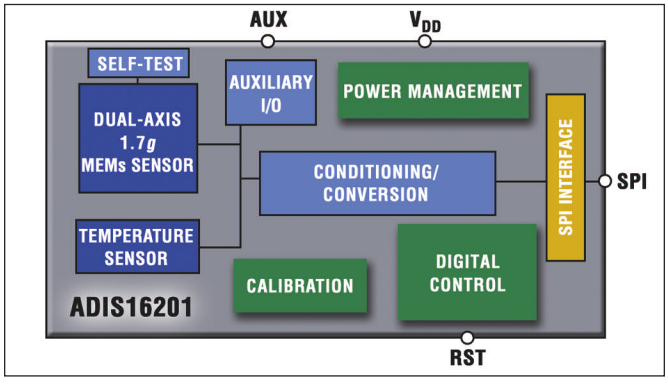
LEADING inside

A series of engineering insights
by Analog Devices.

Highly Integrated, Programmable Single-Component Sensors Solve Problems in Industrial System Design

Sensors have the potential for providing revolutionary improvements in performance, reliability, safety, and cost-of-ownership within industrial system designs. Examples involving inertial sensors include platform stabilization, motion control for industrial machinery, security devices, antenna stabilization, robotics, navigation, mechanical leveling, and many others. However, a gap has long existed between good sensor technology and its implementation within critical industrial systems. Embedding sensor processing within industrial equipment typically requires that the designer have intimate knowledge of the sensor technology to design and implement a signal chain that properly tunes and calibrates a given sensor for its application. For inertial sensors, this typically also requires the capability for motion testing. The system expense of this implementation has created a barrier to more rapid sensor deployment, particularly for customers and applications with moderate production volumes. The problem is worsened by the physical limitations posed by some applications (for instance, embedded vibration analysis) where extreme density, environmental conditions, and remoteness have pushed requirements beyond what is available in standard sensor and signal conditioning components.

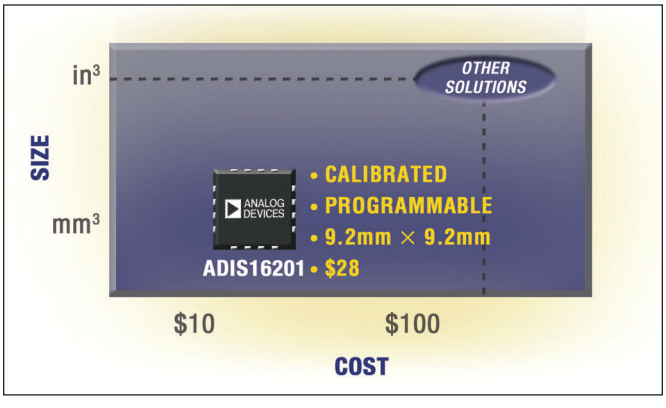
The Analog Devices' *i*Sensor™ product family was created in recognition of this gap in industrial sensor applications. The ADIS16201 *i*Sensor is the first implementation of a new patent pending single-package integration technology. It's the world's first direct output, linear-in-degrees inclinometer that is available as a single component. Incorporating a complete sensor and data processing signal path, the device is both a fully functional programmable dual-axis accelerometer and a dual-axis inclinometer.



A complete dual-axis acceleration and inclination angle measurement system in a single, compact package.

The ADIS16201 provides a gain and offset variability of less than 1%, reduces voltage and mechanical mounting sensitivities, and provides a simple single command interface which allows in-system auto-zero calibration.

It also includes several embedded features, including programmable sample rate, digital filtering, power management, configurable alarms, auxiliary analog and digital I/O, and self-test. This eliminates the need for external circuitry and enables a much simplified system interface, all controlled via an SPI port. Sensor outputs include two axes of ±1.7 *g* acceleration, two axes of ±90° inclination (with accuracy within 0.25°), and temperature. Previously, the same functionality and performance could only be found in devices more than 100× larger, and 10× more costly. The ADIS16201 is available in a small 16-lead laminate-based land grid array (LGA) package, at 1k unit pricing of $28.



With up to 100x size reduction and 10x cost reduction, the ADIS16201 brings embedded sensing to a broader base of customers and applications.

*i*Sensor integration eliminates a key barrier to the advancement of sensor applications in the industrial market by offering unprecedented functionality, programmability, and simplicity to the system designer. The standard programming interface also allows the user to easily tailor the devices to the application, and very quickly move through prototyping, evaluation, and implementation. Now in development are additional *i*Sensor products targeted at embedded vibration analysis and programmable angular rate sensing. For additional product information, visit *www.analog.com/iSensors.*

Author Profile: ***Bob Scannell*** *is the business development manager for the iSensor product strategy at Analog Devices.*

PRY FURTHER AT EDN.COM

For additional photos, and to read more about SuitSat-1, its design and development stages, its champions, and the messages it transmitted, go to www.edn.com/060413pe.

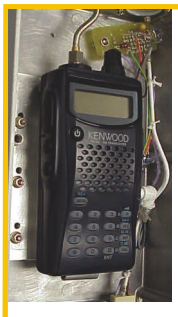
Transmitting from space

A DISCARDED RUSSIAN ORLAN SPACE SUIT SERVES ONE LAST MISSION TO INCREASE AWARENESS OF THE INTERNATIONAL SPACE PROGRAM

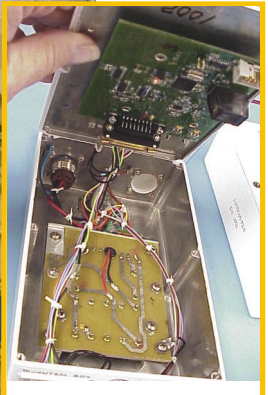
On Feb 3, 2006, the crew of Expedition 12 released the SuitSat-1 into orbit around the Earth. SuitSat-1 is a Russian Orlan space suit that had reached the end of its life, but the cosmonauts added a radio transmitter and sensors to measure temperature and battery power to support one last four- to nine-day mission. Exceeding expectations, for more than two weeks, the space suit captured the attention of the world by acting as a temporary satellite, transmitting recorded messages and telemetry data that students and ham-radio operators could receive. A few weeks after the suit's final mission began, it re-entered Earth's atmosphere and burned up.

The flight team integrated the controller box into the suit and connected it to the switch and transmitter boxes using cables. The controller box provided 12V regulated power from 28V of power to the radio. The controller box housed the EMI filter, the dc/dc converter, and the microcontroller, which read the sensors and managed transmission of the messages and telemetry.

The switch box attached to the helmet by a specially made bracket and connected to the controller box by a cable. The switch box employed three independent safeties to prevent an RF hazard to the deployment team: power, timer 1, and timer 2 switches. The power switch was a latch from the 28V power source to the other two switches that provided a two-pull disconnect from the power source to the radio transmitter. The timer 1 and timer 2 switches enabled a ripple counter that would assert 12V of power to the radio after eight minutes had elapsed; this delay would be enough time for the suit to drift far enough from the station to pose no RF hazard.



The flight team integrated the transmitter box into the suit and connected it to the controller box using a cable. The transmitter box contained an off-the-shelf Kenwood Corp model TH-K2 amateur-radio transceiver with its battery pack removed. The radio mounted on a block of aluminum that acted as a heat sink. The frequency of the radio was 145.99 MHz, and the power output was 500 mW to extend battery life. The radio acted only as a transmitter, with no capability to receive commands.



Three 28V batteries powered the SuitSat-1 controller box. The controller box conditioned and converted the power for the rest of the system components.

TEXAS INSTRUMENTS

POWER MANAGEMENT

Analog Applications Journal

BRIEF

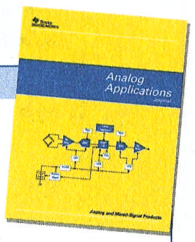
IC Powers White Light LED as Camera Flash

By Scot Lester • Portable Power DC-DC Applications

Introduction

Smart phone, cell phone and PDA manufacturers are incorporating digital camera technology into their products so that the user can use these devices as a camera as well as their intended use. Each of these devices uses a mega-pixel CCD camera, which generally performs poorly in low-light conditions such as indoors, cloudy days, or in the morning or evening. Manufacturers are starting to turn to new high-power, white-light LEDs to provide a photographic flash function for low light conditions. The white-light LED is compact, provides a wide light spectrum output, and is easy to control. White-light LEDs operate at much lower voltages than a Xenon gas discharge tube, which requires hundreds of volts to flash. Additionally, white light LEDs can be turned on continuously to provide lighting for digital movie photography.

One challenge in using white light LEDs is powering them with the wide input voltage range that batteries present. A white-light LED can have a forward voltage ranging from 3.2 to 4.8 volts. This forward voltage range falls in the middle of most battery input voltage ranges, which means the converter needs to be able to step up or step down the input voltage to maintain the forward voltage of the LED.



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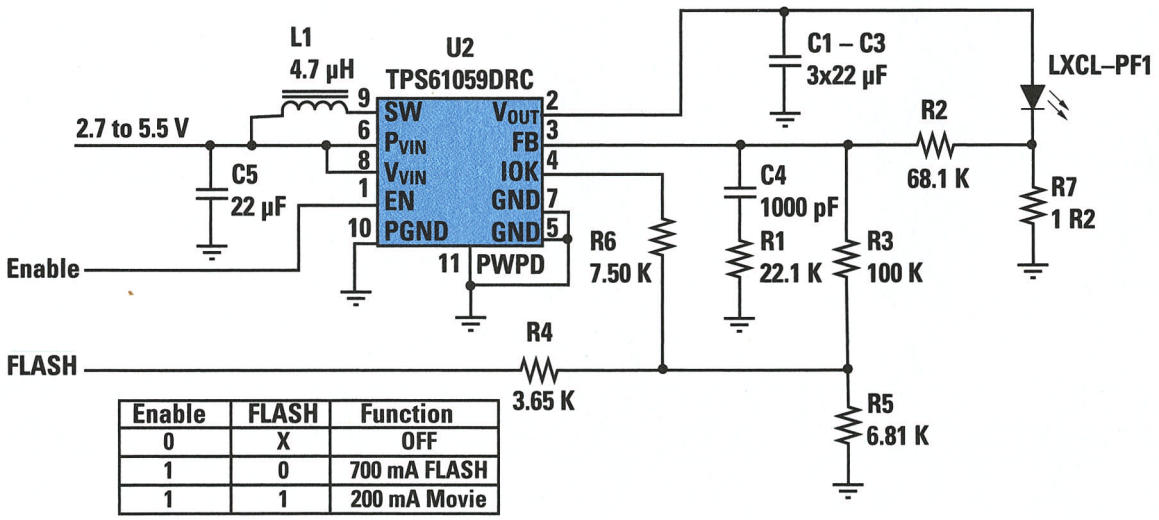
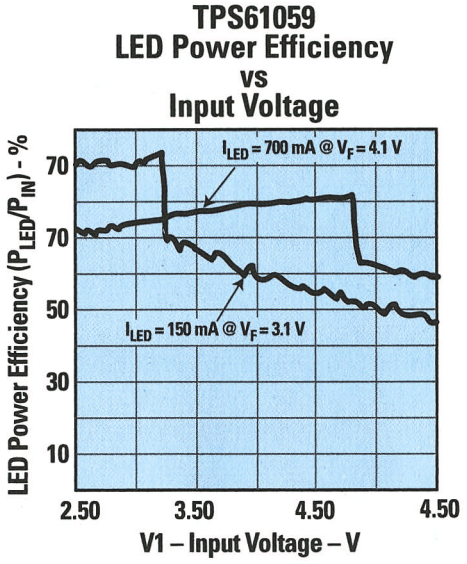
Texas Instruments' TPS61058 and TPS61059 are synchronous boost converters for driving high-current LEDs for movie and flash light applications. The TPS61058 can provide up to 500mA and the TPS61059 up to 800mA of LED current from a 3.3-V source. The TPS6105x family of boost converters has a special down mode that allows it to step down the input voltage when the input voltage is higher than the forward voltage of the LED. Thus, the TPS61058/9 can both step up and step down the input voltage, which allows it to drive a



Enable	FLASH	Function
0	X	OFF
1	0	700 mA FLASH
1	1	200 mA Movie

Figure 1 –TPS61059 based 200mA movie light with 700mA flash

wide range of LEDs from a wide range of input voltages. Figure 1 shows the TPS61059 configured to provide 700mA of LED current for LED flash functions or a constant 200mA of LED current for a movie light function from an input battery voltage between 2.7 to 5.5 volts. Two digital inputs are used to select the mode of operation and the current level for the LED between off, movie light and photo flash. The flash, movie light and soft start current supplied by the TPS6105x are programmed by an external resistor network that allows the TPS6105x to drive a variety of high-power, white-light LEDs.



The TPS6105x achieves up to 93% efficiency in movie light mode and 81% efficiency during high-current flash mode. During shutdown, the device completely disconnects the LED from the input source to prevent draining the battery and consumes a low 100nA of quiescent current.

Additional features are integrated circuit protections such as soft start, thermal shut-down, open LED and shorted LED protections and an integrated anti-ring power switch for low-EMI operation in noise-sensitive applications. All of this is packaged in a 10-pin QFN, which allows for a total solution size of less than 80 square millimeters.

Reference:

1. TPS61058 Datasheet (SLVS572B)

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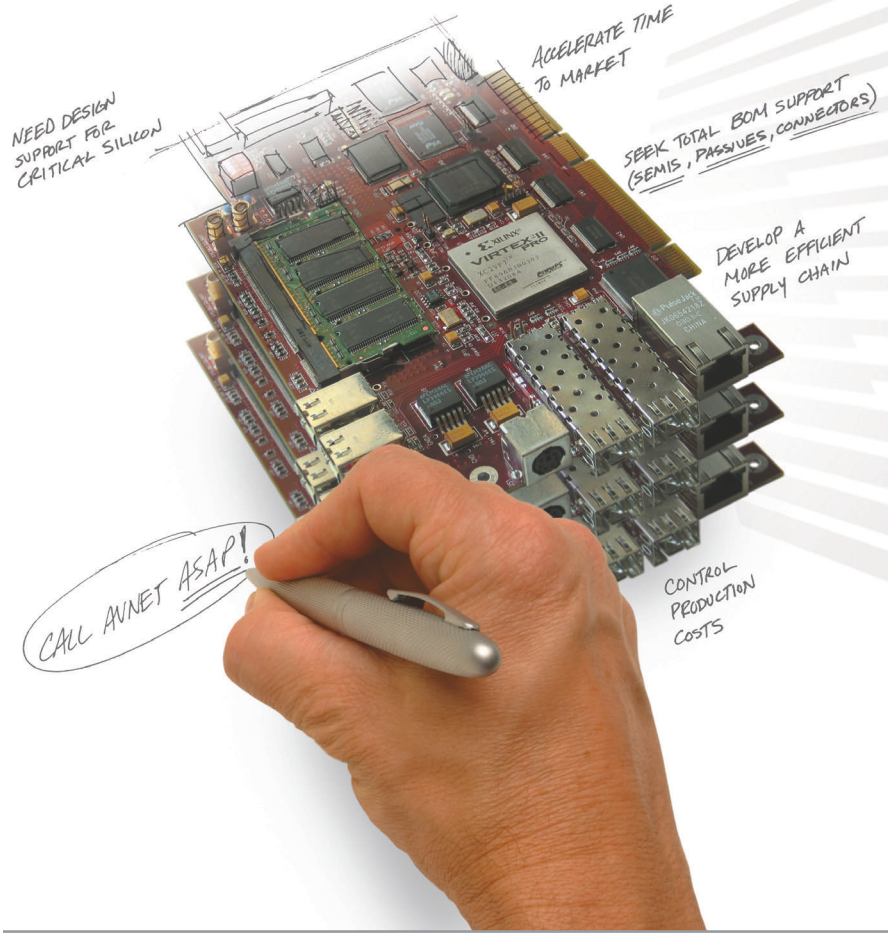

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BY BONNIE BAKER

Tackle noise from three perspectives

You've got noise in your circuit? Where do you look to find it? What source do you consider as the culprit? You can assign your noise to three fundamental categories, each with its own set of noise-reduction methods: device noise, emitted (or radiated) noise, and conducted noise. If you can find the category that your noise problem fits into, the noise-reduction approaches become readily apparent.

Device noise is just what you would assume. Passive components and IC chips generate noise in this category. For instance, passive resistors, whether they are components or within the IC chip, generate a minimum noise that equals $\sqrt{4\times K\times R\times T\times (BW)}$, where K is Boltzmann's constant (1.38×10^{-23}), R is the resistance that you are evaluating, T is the temperature in Kelvin, and BW is the bandwidth in your evaluation. Generally, capacitors and inductors are not noise generators of any consequence, unless you embed them in a switching network. Going forward, you can easily quantify the noise that IC chips generate by examining product data sheets. Reducing resistance or using lower noise IC chips can easily impact the device noise in your circuit.

If you are looking for sources that generate noise, you would next examine the origins of radiated or emitted noise. Radiating sources, such as inductive switching transformers or motors are prime noise-generating suspects. Another, not-so-obvious source of this type of noise is the close proximity of your analog and switching digital pc-board traces. You can also accumulate this type of noise in your system by building circles or ground loops with your traces and unintentionally installing an antenna. Once you understand the source of radiated noise, the solution to your noise-reduction problem will become apparent. For instance, you can increase the distance between analog and digital traces. You can rotate inductive switching systems so that the magnetic fields radiate in a different direction from your sensitive circuitry. But most important, always include an uninterrupted ground plane on your pc board.

If you need a good, clean-running circuit, it is critical that you identify the source or origin of noise in your circuit.

Even after taking all of the noise-reduction precautions, you may still have a noise problem. If you cannot reduce resistances in your circuit or find low-noise devices, you will have conducted noise in your pc-board traces. Conducted noise is simply noise that resides in your traces as a consequence of device noise or radiated noise. A common noise generator is a required switching power supply, which you might need because of its good efficiency. You could also have 50- or 60-Hz noise riding on your pc-board traces, but, in all of these cases, whether the noise originates as device noise or radiated noise, the noise now resides in your pc-board traces as conducted noise. Sometimes, the only approach to this type of noise is to implement noise-reduction filters. You also need to examine all ground- and power-return paths and, once again, a continuous ground plane is preferable. And, by all means, make sure that you are using appropriate bypass capacitors on your active devices.

Your circuit noise will never equal zero. If you need a good, clean-running circuit, it is critical that you identify the source or origin of noise in your circuit. Once you find that source, whether it is device noise or radiated noise, you can implement noise-reduction techniques in your system to bring the circuit noise to tolerable levels. As a preventive measure, you should think about the devices that you select during the design stage. While you work on your layout, use effective layout practices by separating the analog from the digital, eliminating ground loops, and keeping traces as short as possible. Additionally, minimize the effects of radiated noise in your circuit's environment. Finally, when all else fails, good power- and signal-trace filtering may reduce your noise to tolerable levels. A word of caution: Don't go overboard and make your circuit as perfect as you can. On the contrary, design your circuit to be good enough and no better. EDN

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Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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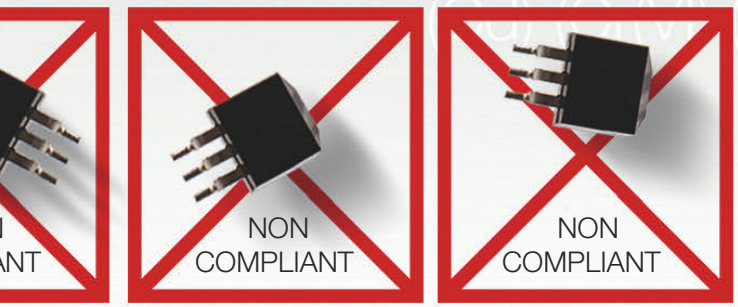

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THE ENVELOPE, PLEASE!

Each year, *EDN*'s Innovation Awards honor outstanding engineering professionals and products. Our Innovator of the Year award recognizes an electronics engineer or engineering team for innovation in product design or technical leadership. The Innovation of the Year awards recognize unique, state-of-the-art electronics products in several categories. This year was no different. The ballots are in, your peers have spoken, and the winners have been revealed.

As usual, the festivities took place in conjunction with the Embedded Systems Conference in San Jose, CA, on April 3. The gala featured a keynote address by August Capital venture capitalist Andy Rappaport, a gourmet menu, and, of course, the opening of the envelopes and unveiling of the winners. To top it all off, *EDN* will donate a portion of the proceeds from the nominations and the awards event to the engineering college or university of the Innovator of the Year's choice. Turn the page to see who took the honors, and please join us in congratulating this year's winners.

EDN's 2005 Innovator/Innovation Program winners

INNOVATOR OF THE YEAR

EinsTimer statistical-timing-tool development team, IBM Research

Corner-based timing is painting IC designers into a corner, but the IBM Research EinsTimer team crafted a potential means of escape. The traditional static approach to ASIC-timing closure, based on "corner," or "case," files, focuses on designing for worst-case scenarios. This pessimistic method leaves much-needed performance on the table. Worse, static tools are proving unable to comprehend the random—and potentially showstopping—process variations that are becoming more numerous and severe as geometries shrink.

With EinsTimer statistical-timing tool, a parameterized, block-based statistical timer, the IBM team proved that statistical timing can be both accurate enough and fast enough for multimillion-gate designs. To do so, the team had to take on and surmount challenges including variational gate and wire modeling, statistical calculations, correlations, software architecture, and incremental timing. The resulting tool reduces pessimism, provides efficient process coverage, and demonstrates the viability of concepts that will become even more important as the design process itself becomes more probabilistic.

ANALOG ICs

VIP50 process and products, National Semiconductor

A brand-new process was the first step in National Semiconductor's development of six new precision op amps that offer as much as 90% power savings over comparable devices. The VIP50 SOI (silicon-on-insulator) BiCMOS process combines highly efficient bipolar transistors; analog-grade MOS transistors; highly matched, low-temperature-coefficient, thin-film resistors; and laser-trim capability. The process dramatically improves the performance of the company's next-generation precision and low-power, low-voltage op amps.

ASSPs AND SOCs

DIB7000-H DVB-H receiver, DiBcom

British research company Visiongain predicts that the DTV-handset market will grow to more than 105 million units worldwide by 2009. In preparation for that popularity boom, DiBcom developed its DIB7000-H chip set, which allows consumers to watch live digital terrestrial television anywhere—on their cell phones, in their cars, and even on their PDAs. The DIB7000-H can demodulate both DVB-H and DVB-T broadcast signals, and it can process a 24-Mbps digital signal in an error-free manner even when the receiver is traveling at 150 mph. The chip set incorporates a circuit block for IF (intermediate-frequency) and baseband inputs, enabling its interface to very-low-power RF tuners.

COMMUNICATION ICs

AGN300 802.11 a/b/g True MIMO chip set, Airgo Networks

The Holy Grail of the connected home remains a "no-new-wires" way to move rich data streams. Airgo Networks claims that its newest chip set provides the speed and reliability necessary to enable the distribution of content—such as media-rich Internet, large files, video, IPTV service, music, photos, and games—across a wireless network without compromises in performance and remaining 100% compatible with 802.11b, 11g, and 11a Wi-Fi.

Offering connection speeds that the company purports are faster than 10/100 Ethernet, the chip set eliminates the need for unsightly and inflexible wired connections between devices in the home, such as routers, laptops, PCs, set-top boxes, game consoles, and TVs. In addition, Airgo's third-generation technology makes the wire-free office a reality.

DIGITAL ICs/ PROGRAMMABLE LOGIC

Fusion mixed-signal FPGA, Actel

Fusion combines mixed-signal-analog capabilities with large amounts of flash memory and an FPGA fabric. The Fusion PSC (programmable-system chip) brings the benefits of FPGAs to applications that discrete analog-component and mixed-signal-ASIC suppliers have historically served.

The technology takes advantage of a high-isolation, triple-well process, along with Actel's ability to support high-voltage transistors. Fusion peripherals include hard analog IP (intellectual property) and both hard and soft digital IP, such as Actel's CoreMP7 and 8051-based microcontroller cores. Cores communicate across the FPGA fabric by means of a layer of soft gates called the Actel Fusion Smart Backbone. More than a bus interface, the backbone integrates a microsequencer within the FPGA fabric, which configures the individual peripherals and supports low-level processing of peripheral data.

DIGITAL-SOC INTELLECTUAL PROPERTY

Dynamic Point-to-Point technology, Rambus

One of the most frustrating roadblocks that today's engineers face is balancing the necessary trade-offs between memory performance for capacity and expandability. Rambus' DPP (Dynamic Point-to-Point) technology aims to eradicate performance deficiencies inherent in previous approaches.

The DPP inventors anticipated the

BEST CONTRIBUTED ARTICLE OF 2005

"Minimizing switching-regulator residue in linear-regulator outputs," by Jim Williams, Linear Technology, Dec 5, 2005. To read the article, visit www.edn.com/article/CA6288040.


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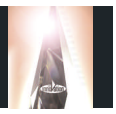

future direction of the market and implemented high-speed differential signaling. DPP technology allows designers to maximize memory capacity without compromising the signal-integrity benefits of point-to-point signaling. DPP technology allows PCs or home servers to use a single memory module at full bandwidth but with an option for a second module upgrade on a fixed datapath. This feature enables eight times greater memory bandwidth than previous technologies for consumer, multimedia, and computing systems—and still supporting traditional modules and new-application form factors.

EDA (DESIGN AND IMPLEMENTATION)

EinsTimer statistical-timing tool, IBM Research

After winning accolades and finally the best paper award at the 2004 DAC (Design Automation Conference) for advancements in statistical-timing-analysis research, IBM Research made its EinsTimer statistical-timing tool commercially available in 2005. The tool gives a truer account of circuit performance than static tools, which corner files drive. These corner files sometimes provide pessimistic design scenarios. The EinsTimer statistical-timing tool seemingly debunks the long-held myth that accurate statistical analysis of multimillion-gate designs is computationally intractable. For more details, see "IBM makes EDA play, offers commercial statistical-timing tool" at www.edn.com/article/CA605769.

EDA (VERIFICATION AND ANALYSIS)

FireBolt full-chip thermal-analysis software, Gradient Design Automation

Introduced in June 2005, Gradient Design Automation's FireBolt IC thermal-analysis tool is unique in that it addresses thermal analysis from an IC-design perspective rather than from a packaging or systems perspective. Heat worsens transistor leakage, so by gaining a better understanding of on-chip thermal issues, users can better check their designs and thus see how their overall systems conform to low-power requirements. For more details, see "EDA start-up targets IC thermal hot spots" at www.edn.com/article/CA607747.

EMBEDDED SYSTEMS

XPort AR embedded-processor module, Lantronix

The Lantronix XPort AR is the first embedded-device server that goes beyond simple network connectivity to provide manufacturers with intelligence at the network edge by incorporating standards-compliant information-transport and security protocols. The XPort AR module includes a complete embedded computer and an Ethernet 10/100 interface, along with an onboard network operating system and Web server in an RJ45 package about the size of two sugar cubes. You can use the fully integrated XPort AR as a device's CPU, allowing developers to add their own device-specific intelligence through an API (application-programming interface). The POE (power-over-Ethernet) pass-through feature eliminates the need for power cables to the device, making the XPort AR the first fully IEEE POE standards-compliant embedded-device-server module.

POWER ICs

STw4141 dc/dc-converter IC, STMicroelectronics

STMicroelectronics' STw4141 dc/dc converter allows, for the first time, generation of two output voltages using a single external coil, thereby allowing parts-count reduction in both pc-board area and manufacturing cost in applications that require two power rails. The device supplies digital baseband and multimedia processors in portable-system applications, such as mobile phones, digital still cameras, and PDAs, which operate under tight pc-board-area, cost, and power-consumption constraints.

Typically, processors that these applications use require separate supplies for the core, which can run on voltages as low as 0.9V in new designs, and the I/O circuitry. Current practice is to use two standard step-down dc/dc converters, each of which requires a coil, two or more external capacitors, and, in some cases, external resistors to set the output voltage. All dc/dc converters require an external coil, which significantly impacts the BOM (bill-of-materials) and the application costs. With its single-coil/dual-output architecture, the STw4141 cuts the BOM cost by as much as 40% and reduces pc-board size by 30%, compared with previous standard-supply approaches. For example, you can implement a complete STw4141 design using only 56 mm^2 of pc-board area, compared with approximately 80 mm^2 for the best alternative approaches.

POWER SYSTEMS AND MODULES

LTM4600 high-power dc/dc micromodule, Linear Technology

Linear Technology's LTM4600 is the first high-power dc/dc module that meets the spacing and assembly requirements of densely populated boards, such as advanced embedded systems. This encapsulated µModule dc/dc power supply comes in a 15×15×2.8-mm LGA package. This complete power supply is smaller than most FPGAs and processors. Because it has only a 2.8-mm profile, you can place the LTM4600 on the backside of a board without adding significant thickness to the end product.

The µModule is rated for 20 and 28V input operation. The output voltage is adjustable with a single resistor from 0.6 to 5V. The device can deliver as much as 10A of output current and offers fast transient response to fast-changing load-current transients.

PROCESSORS

CT3600 multicore DSP, Cradle Technologies

Cradle Technologies' CT3600 multicore devices comprise two computational quads that symmetrically organize eight to 16 digital-signal processors with four to eight general-purpose processors targeting multimedia applications.

To support high data throughput for the multiple cores, the CT3600 architecture employs a three-tier memory hierarchy, a wide and flexible DDR SDRAM interface, a 64-bit internal global bus, and several dedicated I/O and DRAM DMA engines. The smart I/O subsystem comprises as many as 18 pin groups of eight pins each, which a PLA block and a series

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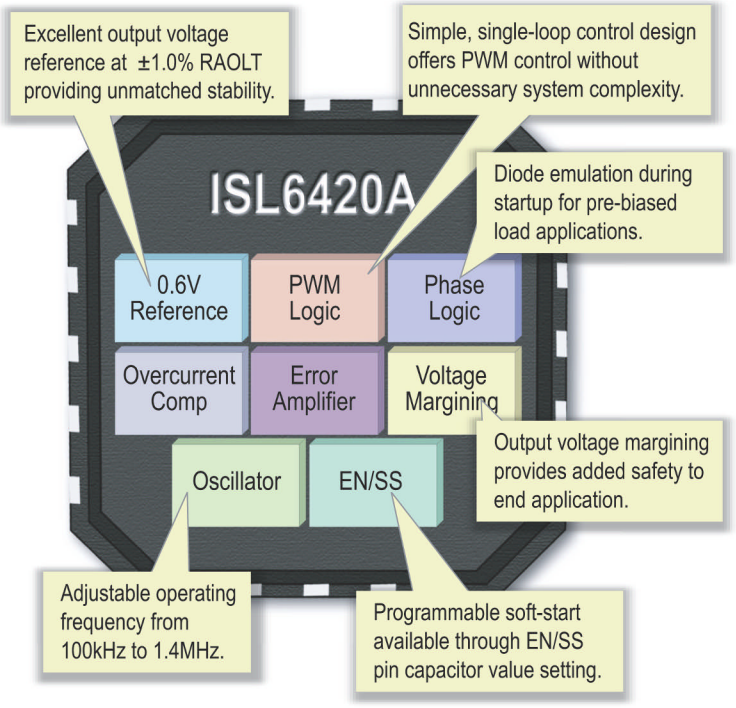
Intersil knows that different applications have different design needs. That's why we've created the ISL6420A wide V_{IN} Step Down Controller. In addition to the flexibility to support multiple input voltages, this device combines control, output adjustment, monitoring and protection into a single package.

The ability to address a wide input voltage range of 4.5V to 28V gives the ISL6420A unmatched flexibility for use in most general purpose applications. It also has resistor-selectable switching frequency from 100kHz to 1.4MHz. Add all this up and Intersil has made choosing the right switching regulator for your design...well, like a day at the beach.



Key Features:

- Operates from 4.5V to 28V input
- Excellent output voltage regulation with 0.6V internal reference with ±1.0% ROALT
- Resistor-selectable switching frequency from 100kHz to 1.4MHz
- Voltage Margining and External Reference Tracking
- Output can sink or source current
- Lossless, programmable overcurrent protection using upper MOSFET's rDS(on)
- Programmable soft-start
- Simple single-loop control design
- Fast transient response
- High-bandwidth error amplifier
- Full 0% to 100% duty cycle
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of FIFOs support. Each pin group is fully programmable for data, control, or a combination of the two.

SENSORS AND COMPONENTS

ADNS-6010 laser-based optical-mouse sensor, Avago Technologies

PC gamers demand the highest accuracy and most responsive tracking from their input devices. A fraction of a second's delay in response or a minor inaccuracy in position could mean the difference between victory and defeat.

To help address this need, Avago Technologies developed a high-performance, laser-based optical-mouse sensor primarily aiming at gaming mice. The sensor allows manufacturers to offer mice that are ideal for the requirements of today's highest performance PC games. For FPS (first-person-shooter) games, the user wants extreme efficiency in hand movement and cursor responsiveness. Pro gamers use special surfaces, such as metal and slick plastic, to assist their hand movements.

SOFTWARE

LabView 8, National Instruments

LabView 8 is an upgrade of National Instruments' LabView graphical-development platform. The tool offers distributed intelligence and a suite of new capabilities that allows engineers and scientists to easily design, distribute, and synchronize intelligent devices and systems. The software features a new project-based environment for developing and managing large-scale applications, as well as the latest in Express technology for simplified instrument control.

Together with significant updates to the LabView real-time module, LabView FPGA module, LabView PDA module, and LabView data-logging and supervisory control module, LabView 8 presents a simplified, scalable interface for communicating with and synchronizing remote intelligent devices and systems, such as real-time processors and FPGAs.

TEST AND MEASUREMENT (APPLICATION SPECIFIC)

N4903A high-performance serial BERT with jitter-tolerance testing, Agilent Technologies

The next generation of gigabit serial-bus standards is approaching. Data rates of 5 Gbps and beyond will cause signal-integrity and jitter issues during design and characterization of chips and systems. Agilent Technologies' N4903A high-performance serial BERT (bit-error-ratio tester) provides complete jitter-tolerance testing for the smartest characterization of gigabit-per-sec serial devices.

The N4903A offers complete, built-in, and calibrated jitter-composition measurement for stressed-eye testing of receivers to 12.5 Gbps. Automated and compliant jitter-tolerance testing allows quick and accurate characterization for all popular serial-bus standards.

TEST AND MEASUREMENT (BROAD APPLICATION)

WaveExpert near-real-time digital oscilloscope, LeCroy

Engineers who characterize semiconductor devices, high-speed clocks, and other electronic and optical devices that produce high-frequency signals and fast serial-data streams have for many years used sampling oscilloscopes. They do so, in part, because real-time scopes, though they have other advantages over sampling scopes, lack the bandwidth to make accurate measurements on ultrafast signals. Sampling scopes have their own problems, though, which make them much less user-friendly than real-time scopes. To combine the best features of both instrument classes, LeCroy has created a new category—NROs (near-real-time oscilloscopes), which combine sampling scopes' high-bandwidth-measurement capability with real-time scopes' long memory and throughput speed.

The WaveExpert NRO's CIS (coherent interleaved sampling) changes the way sampling occurs. CIS employs a data-acquisition technique that uses a phase-locked sampling strobe that is referenced to a user-supplied or recovered clock. This feature allows the WaveExpert, at 10M samples/sec, to acquire data at least 50-times as fast as the fastest sequential-sampling scope. The WaveExpert can also acquire a minimum of 1000 times as many data points. EDN

On our dedicated Innovation Web page, you will find not only more in-depth descriptions of our nominees and winners, but also a photo gallery of the awards event, a history of our Innovation Awards, and details on next year's program.
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Intersil Battery Charger ICs

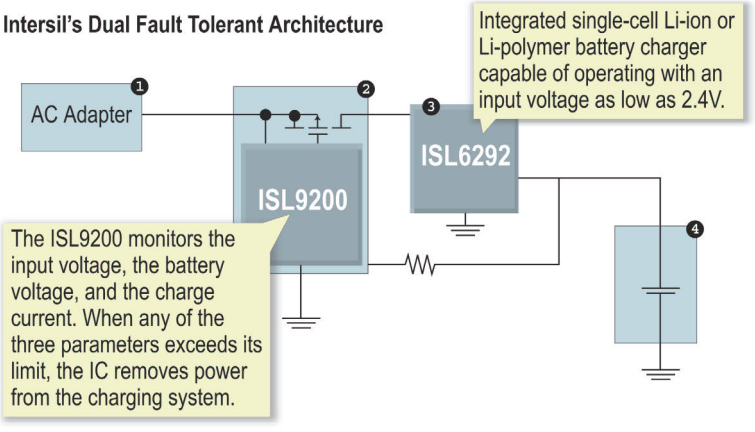
High Performance Analog

The Scariest Thing Inside Your Handheld Should Be Your Pictures

There **is** a real monster out there. Protect your customers from the onslaught of counterfeit and non-OEM battery packs with Intersil's innovative Dual Fault Tolerant charging system. Our integrated triple-level protection approach reduces components and cost while improving design flexibility and system reliability.

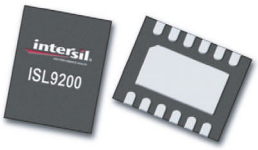
The ISL9200 is a Fault Protection IC optimized to provide redundant safety protection in Li-ion battery charging systems. Together with the ISL6292 Battery Charger IC, Intersil's integrated battery charging system will keep even a counterfeit battery within safe operating limits.

Intersil's Dual Fault Tolerant Architecture



Dual-Fault FMEA (Failure Mode and Effects Analysis)

POTENTIAL FAILURES				Consequence of Dual Failure
❶	❷	❸	❹	
●	●			❸ will fail but the protection module in the battery pack will protect the battery cell.
●		●		Both ❷ and ❹ will protect the battery cell.
●			●	❸ will limit the battery voltage. ❷ has an additional level of protection.
	●	●		The protection module in the battery pack protects the cell.
	●		●	❸ will limit the battery voltage to 4.2V, within 1% error.
		●	●	❷ will sense an over voltage case and remove the power from the system.



- User programmable overcurrent protection threshold
- Input overvoltage protection in less than 1µs
- Battery overvaltage protection
- High immunity of false triggering under transcients
- High accuracy protection thresholds
- Warning output to indicate the occurrence of faults
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SIMPLE

BY DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

WITH A SUITABLE PROTOCOL, SUCH AS ZIGBEE, SENSORS THAT DON'T HAVE A LOT TO SAY OR HEAR NEEDN'T CONSUME MUCH ENERGY TO KEEP IN TOUCH. SOMETIMES, AN ALKALINE CELL CAN PROVIDE ALL THE POWER THEY NEED FOR AS LONG AS A DECADE.

NETWORKS will free many sensors from wires

The folks at the ZigBee Alliance, the industry organization driving ZigBee WPAN (wireless-personal-area-networking) technology, mean it when they say that they've learned valuable lessons from the miscues of the proponents of another such technology: Bluetooth. Bluetooth is now well-established and is here for the long haul—at least in the narrowly targeted market niche of wireless headsets for cell phones and portable entertainment devices. However, its advocates' early misadventures with creeping elegance almost sank the standard while it was still in its formative stages and certainly delayed its widespread deployment. The lesson: In this era of wireless everything, trying to be all things to all people is an almost-sure-fire recipe for failure.

ZigBee's creators based it on the IEEE 802.15.4 wireless-communication standard and named it for the zigzag "dance" that honeybees use to communicate the location and distance of sources of nectar. It is a technology that knows its place. It targets sensors, but not even all sensors—just low-speed devices that need to send data no more often than about once per second. There are several reasons for this focus: If a sensor is to be wireless, eliminating the signal wiring doesn't accomplish much if power wiring is still necessary. So, at least initially, most ZigBee sensors will be battery-powered. Most sensors are small, suggesting that battery-powered versions must not be much larger. Therefore, the batteries need to be small, and small batteries store only modest amounts of energy.

To achieve acceptable battery life, the sensors and their communication circuits must therefore use power sparingly. The most straightforward way to achieve this goal is to minimize the duty cycle—in this case, the percentage of time that a device is on the air. When not communicating, the device is in a low-power sleep mode. Most sensors generate messages that last only a few milliseconds at 802.15.4's data rate of 250 kbps at 2.4 to approximately 2.48 GHz. The rates are 40 and 20 kbps, respectively, at 902 to 928 MHz and 868 to 870 MHz. Because the

AT A GLANCE

- ZigBee is a low-power, relatively low-speed wireless-personal-area-networking technology that aims at sensors.
- By not attempting to be all things to all people, ZigBee is getting a warm reception.
- Alkaline batteries will power most initial ZigBee devices. However, energy harvesting, which scavenges small amounts of energy from the environment, such as from light and vibration, offers the hope of eliminating batteries from some ZigBee applications.
- ZigBee will make slow and steady inroads into industrial applications. A conservative approach is warranted, because demonstrating the reliability of a low-speed protocol takes time.

transition from sleep mode to data transmission takes approximately 15 msec, a sensor that sends, on average, one message per second usually operates at a duty cycle of 2% or less in the 2.4-GHz band and little more in the 868- and 915-MHz bands. Many sensors send messages much less often. For these sensors, the duty cycle is so low that the battery life can essentially equal the battery's shelf life: as long as 10 years for alkaline cells.

SOLID RATIONALE

The rationale for having a standard for networks of wireless sensors is a lot more serious than, "Everything is going wireless these days, so why not sensors?" Many applications involve large numbers of sensors. In such cases, the cost of mounting and wiring the sensors can greatly exceed the cost of the sensors themselves. Of course, ZigBee doesn't address the not entirely facetious issue of having sensors fly unaided to and then perch at the spot where you'd like them mounted, so part of the cost of sensor installation remains even with wireless sensors.

ZigBee targets a wide range of building-automation, industrial, medical, and residential-control and -monitoring applications. Applications that require IEEE 802.15.4's interoperability, RF characteristics, or both can benefit from ZigBee. Examples include: lighting controls; remote reading of electric, gas, and water meters; wireless smoke- and carbon-monoxide detectors; HVAC (heating, ventilating, and air-conditioning) and environmental controls; home security, intrusion, and motion detectors; blind, drapery, and shade controls; medical sensing and monitoring; universal remote control of set-top boxes that include home-control functions; and industrial and building automation. The first ZigBee products—for home-control, -safety, and -security applications—should appear in stores by midyear. Packaging for these products will prominently display the ZigBee logo (**Figure 1**).

The ZigBee specification overlays network-, security-, application-framework-, and application-profile layers atop 802.15.4's PHY (physical) and MAC (media-access-control) layers (**Figure 2**). The 802.15.4 standard's 2.4-GHz version is usable in unlicensed bands worldwide. It specifies O-QPSK (offset-quadrature-phase-shift-keying) modulation with half-sine pulse shaping, which is equivalent to MSK (minimum-shift keying). Each symbol carries 2 bits, channel spacing is 5 MHz, and there can be as many as 16 channels. Although devices do not frequency-hop among the channels, selecting channels can often optimize reception. To minimize interference among the networked devices and—in conjunction with other techniques—to enhance data security, the 2.4-GHz version also uses 2M-chip/sec DSSS (direct-sequence-spread-spectrum) coding. The less-than-1-GHz versions use BPSK (bipolar phase-shift keying) with root-raised-cosine pulse shaping and, in the 915-MHz version, 2-MHz channel spacing. (The 868-MHz band has room for only one channel.) BPSK transmits only 1 bit per symbol. In the 868-MHz (largely European) and the 915-MHz (western hemisphere plus Australian) versions, respectively, the data rates are 20 and 40 kbps, and the DSSS chip rates are 300k and 600k chips/sec.

ZIGBEE DOESN'T ADDRESS THE NOT ENTIRELY FACETIOUS ISSUE OF HAVING SENSORS FLY UNAIDED TO AND THEN PERCH AT THE SPOT WHERE YOU'D LIKE THEM MOUNTED.

Figure 1 Like the standard it represents, the easily recognized ZigBee logo presents a simple, straightforward message to the customer. This version appears on the packages of consumer products that operate in the 2.4-GHz band. Versions also exist for products that operate in the less-than-1-GHz bands (courtesy ZigBee Alliance).

In all three bands, the 802.15.4 MAC layer uses CSMA/CA (carrier-sense multiple access with collision avoidance)—fundamentally the same mechanism that Ethernet uses. A device that wants to transmit wakes from sleep mode and first listens for activity on its channel. If it detects activity, it goes back to sleep for a random interval and then reawakens and again listens for activity. If it hears none, it sends its message. Of course, two or more devices can be listening simultaneously—in preparation for sending data. Several of them might incorrectly conclude that the coast is clear and begin transmitting at the same time.

MESSAGE GETS THROUGH

According to ZigBee Alliance members, because of the DSSS coding, the chances are good that the messages will get through despite the interfering transmissions. But if a sender does not receive an acknowledgment, it goes back to sleep for a random period and then tries again to send its message. The obvious problem with CSMA/CA is its nondeterministic

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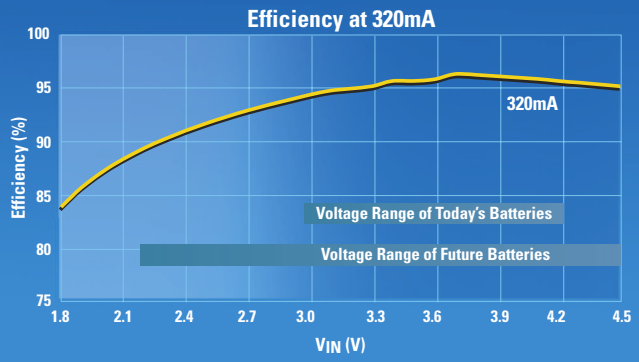

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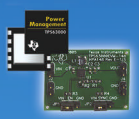

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latency. That is, system designers can't be certain how long any message will take to reach its intended recipient. However, as Ethernet proved decades ago, when it was much slower than it is today, the scheme works admirably in many common applications. Also, the longer you can wait for a response, the greater the likelihood that the system can meet your needs.

For those who must have deterministic latency, however, the IEEE standard provides two additional mechanisms that together guarantee it within a tight tolerance. Beacons are special messages that are permitted in certain ZigBee network topologies. Beacons wake up client devices, which listen for their address and go back to sleep if they don't receive it. It is possible to designate times, separated by multiples of 15.38 msec to a maximum of 252 sec, when the devices must listen for beacons. A beacon can announce a superframe, another kind of special message, which provides 16 time slots between beacons. During these slots, designated devices receive contention-free network access.

OVER-THE-AIR SOFTWARE DOWNLOAD IN WIRELESS-SENSOR NETWORKS

By Larry Friedman, Texas Instruments

A characteristic of wireless-sensor networks is their lack of physical connectivity (wiring) between the sensor/actuator array and the network. Although the absence of wires simplifies placing hardware in hard-to-reach locations, when software upgrades become necessary, you can't fall back on wires for downloading the new code. OAD (over-air downloading) solves this problem, but you must address several issues to successfully implement OAD. Texas Instruments supports OAD with the Chipcon Wireless OAD product.

In a layered transport architecture, such as ZigBee/802.15.4, support for a scheme such as OAD is a matter of writing an application. The layer at which this application exists is a design choice, and the choice has implications. For example, writing OAD support as a ZigBee application allows use of the entire stack as infrastructure to support multihop routing, thus eliminating the need for proximity between the source and the target. Using a MAC (media-access control)-layer application would sacrifice this network-routing support to reduce the size of the file-transfer-support code. All methods require a repository of some size to store the downloaded code.

OAD support must be fail-safe. It must be robust enough to survive transmission errors, interrupted file transfers, and interrupted enabling of the new code–that is, interrupted flashing of the new image. If any of these steps fail, the device's remaining software must be able to recover. The file transfer itself must also be secure.

To deal with interrupted transfers, the software must meet two conditions. First, the software entity that supports the transfer on the target must remain intact until the transfer succeeds. Second, you cannot expect the portion being transferred to operate until the transfer is complete. These two requirements together imply that the downloaded-code repository must store the transferred portion of the new code, and this portion cannot disrupt the code that implements the transfer. If the code meets these conditions, the code supporting an interrupted transfer can retry the transfer at its next opportunity.

MITIGATING ERRORS

Frame-check sequences in the ZigBee stack mitigate transmission errors. Various layers each use these sequences to provide their own level of guaranteed-delivery support. In addition, you can apply a mechanism such as CRC (cyclic redundancy check) over the entire transferred file for a final check and to detect incomplete flashing of the newly downloaded code entity. Both ZigBee and the 802.15.4 MAC and PHY (physical) layers also support file-transfer security.

The file-upgrade-distribution architecture addresses how the target platform "knows" that an upgrade is necessary. TI's approach uses a managed client-server technique in which a management tool determines the code versions on each platform and assigns client and server roles depending on the platform's location and the code's availability. The penetration of the new code increases as more target platforms receive the code. Each upgraded client can then become a server to another client. The management tool assigns these roles on the fly. This technique works because these networks, though often large, are well-defined and reasonably stable. A management tool makes sense in this environment.

AUTHOR'S BIOGRAPHY

Larry Friedman is a software-design engineer for low-power wireless devices at Texas Instruments Inc. He holds a bachelor's degree in psychology from Duke University (Durham, NC) and a PhD in psychology and computer science from the University of Maryland (College Park, MD). For the last 15 years, he has worked in design, development, and firmware architecture for small to midsized embedded systems and wired and wireless distributed-control and sensor/actuator platforms.

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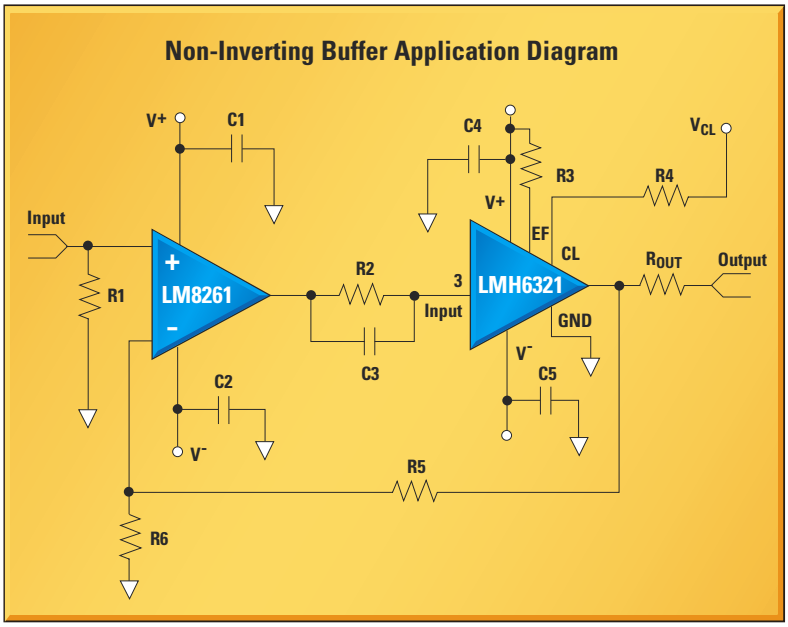

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The ZigBee Alliance's slogan or position statement is "Wireless control that just works." From all indications available at this early date, ZigBee is living up to that slogan, but it took *a lot* of work and technology to make wireless control "just work." Version 1.0 of the ZigBee specification (**Reference 1**), which you can download at no charge from the Alliance Web site, runs 426 pages, and the PDF file fills almost 8 Mbytes. Moreover, the spec does not deal with the PHY and MAC issues that the 5-Mbyte, 679-pg IEEE 802.15.4-2003 standard covers (**Reference 2**). In other words, even though ZigBee is a well-focused, low-power, relatively low-speed protocol, its developers have invested a huge amount of effort to ensure that users find that it works without wheel-spinning or fuss.

One aspect of wireless-communication protocols that should concern all potential users is data security. Although you may wonder how much harm an interloper outside your house could do if he were able to, say, find out—or even change—the setting of your downstairs thermostat, the stakes are a lot higher in industrial and commercial applications. And, even in the home-thermostat example, the interloper might be able to cause very expensive mischief, such as frozen water pipes. ZigBee's DSSS coding provides a first level of security, but ZigBee also uses a security-toolbox approach to ensure reliable and secure networks. Access-control lists, packet-freshness timers, and 128-bit encryption based on the NIST (National Institute of Standards and Technology)-certified Advanced Encryption Standard help to protect data transmission and ZigBee networks themselves.

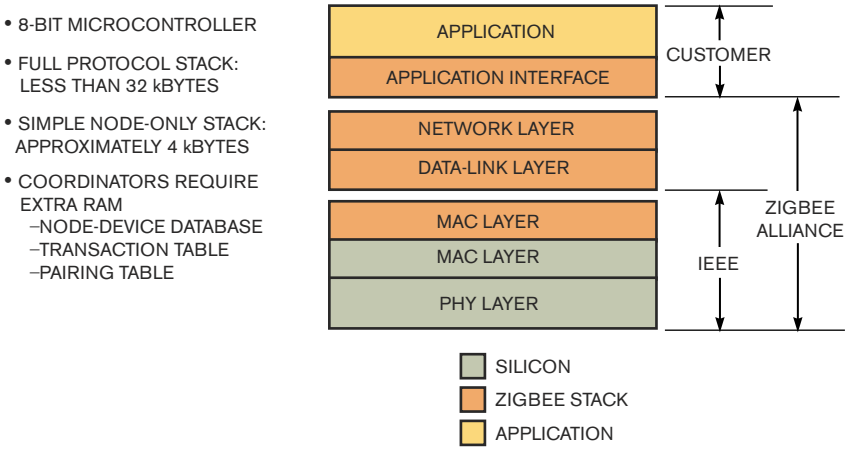

Figure 2 ZigBee is a layered protocol. IEEE standard 802.15.4 governs the bottom (green) layers. The ZigBee specification governs the middle (orange) layers. The customer controls the topmost application layer (gold). Orange denotes the layers that constitute the stack contained in ZigBee-platform ICs (courtesy ZigBee Alliance).

ZIGBEE PROFILES

A cornerstone of ZigBee is the profile, an example of which is home-control lighting. The initial version of this pro-

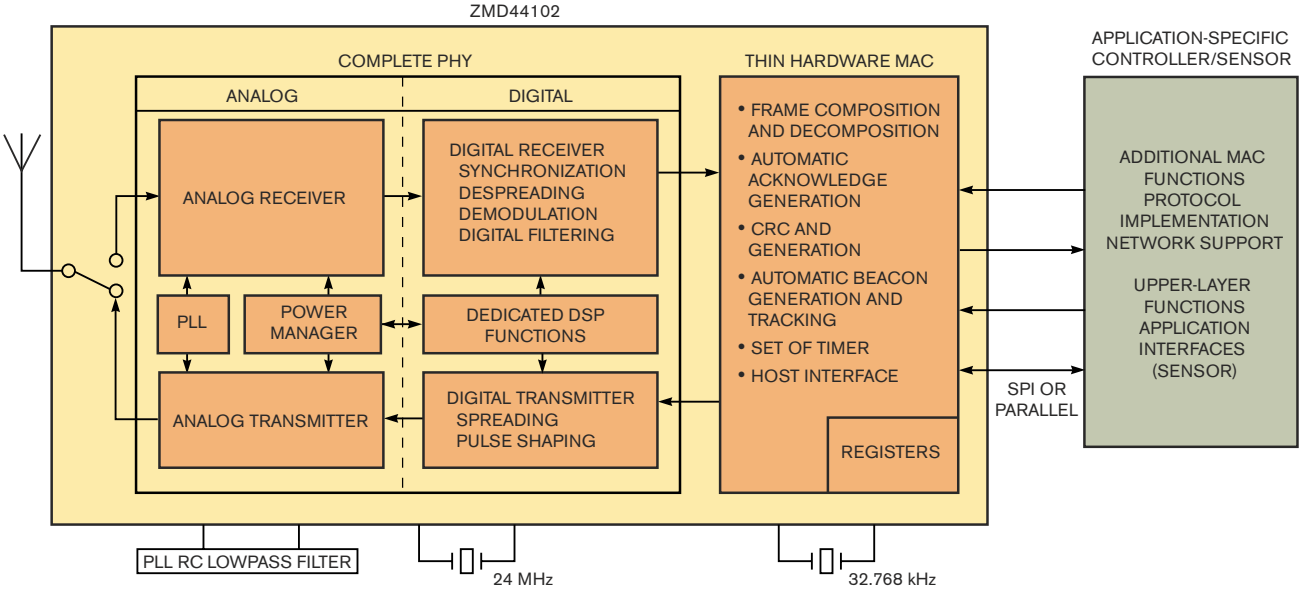

Figure 3 Though it applies to a less-than-1-GHz device, this platform is typical of single-chip ZigBee platforms. The ZigBee platform is on the left. The block at the right contains the application-specific functions (courtesy ZMD).

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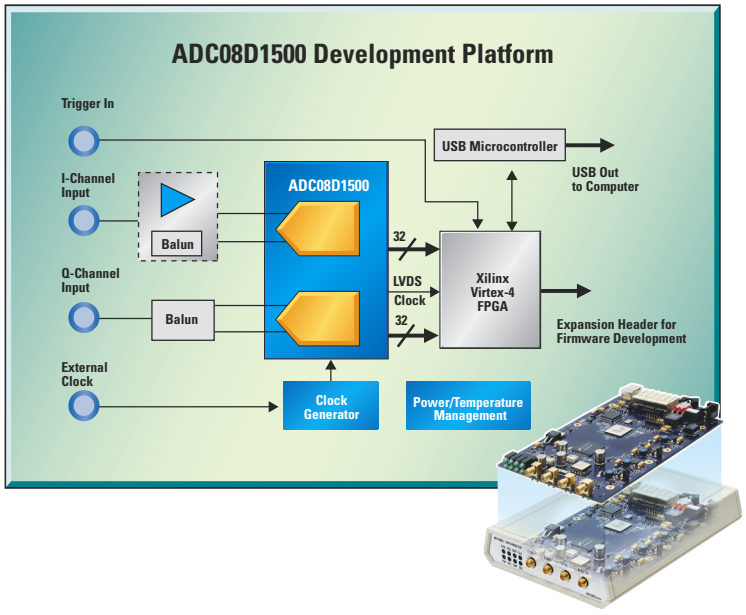

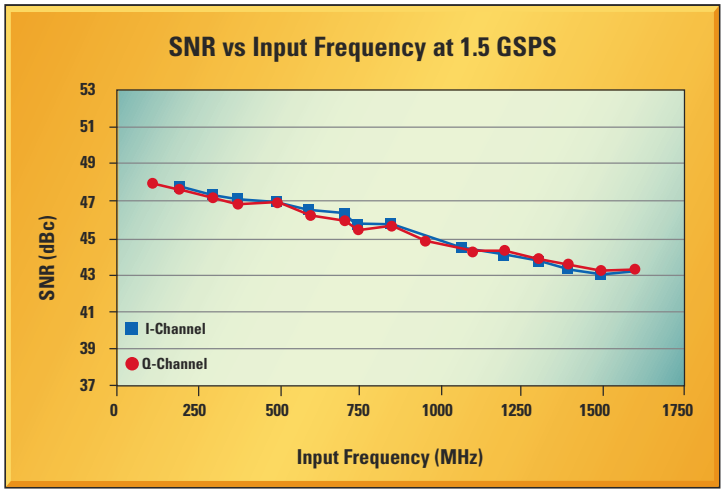

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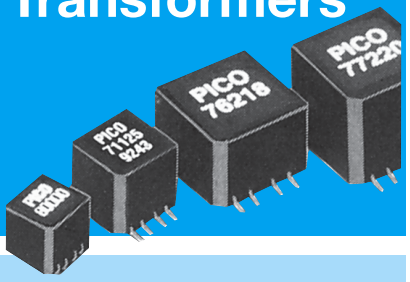

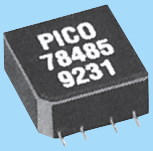

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file permits a series of six device types to exchange control messages to form a wireless home-automation application. These devices exchange well-known messages to effect control, such as turning a lamp on or off, sending a light-sensor measurement to a lighting controller, or sending an alert message if an occupancy sensor detects movement. Another example is the device profile that defines actions common to ZigBee devices. For example, wireless networks rely on autonomous devices' ability to join a network and to discover other networked devices and the services they offer. The device profile supports device and service discovery.

The ZigBee specification allows device manufacturers to establish proprietary profiles that implement features you won't find in other manufacturers' products. The Alliance intends, however, that such proprietary features shouldn't prevent devices from different manufacturers from operating together in networks. That is, devices that implement proprietary profiles should still perform their basic functions even if other network devices lack features that the proprietary devices need to implement their unique capabilities.

The ZigBee-platform portion of a ZigBee device implements the RF- and baseband-communication functions. Although multichip ZigBee platforms are currently common, expect the most common platform configurations to soon use one chip—not the identical design in all platforms, but a single chip from any of several suppliers (**Figure 3**). Different manufacturers' platform chips, which are expected to cost approximately $5 each in production quantities, will differ in detail and depending on whether the intended use is at 2.4 GHz or at 868/915 MHz. Despite these differences, however, the ICs will perform all of the functions that are related to ZigBee but aren't specific to particular applications. Besides the RF functions, these chips will contain a processor and sufficient nonvolatile rewritable—that is, flash—memory to hold the ZigBee software stack.

Software, of course, plays a central role in ZigBee, and you can make a good case that no implementation of a software-dependent protocol is complete without a way of performing software upgrades. However, in a wireless environment, such upgrades present special problems that designers must work through in advance of deployment (see **sidebar** "Over-the-air software download in wireless-sensor networks").

Except in high-volume applications, for which it sometimes makes sense to integrate the application-specific functions with ZigBee-platform functions, expect the application-specific functions to reside on a second chip. An industry

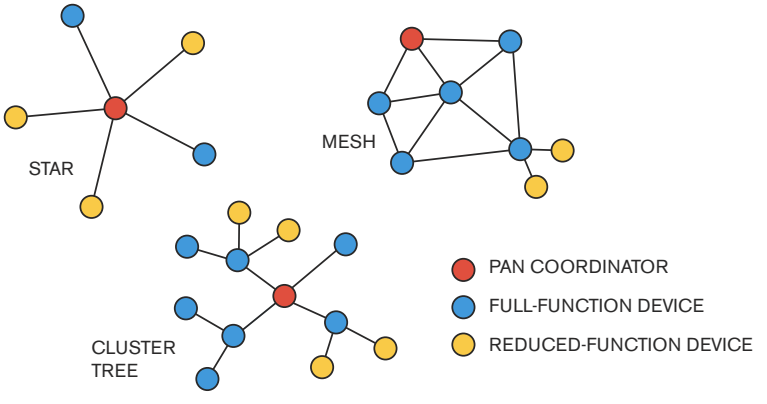

Figure 4 Although the mesh topology is most closely associated with ZigBee, the ZigBee specification offers two other alternatives and specifies which ZigBee features are available in each. Note that, in ZigBee, a message can make multiple hops to reach its destination (courtesy ZigBee Alliance).

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is developing to provide ZigBee-platform modules, which contain the platform chip and additional circuitry, such as clock crystals, for example, to support that chip. Some of these modules provide features for prototyping the application-specific portion of the final device; others that target use in volume production lack prototyping features.

DIFFICULT QUESTION

A frequently asked question about ZigBee is: "What is the range of the transmissions?" Although the short answer is 10 to 100m, it is much easier to ask this question than to answer it. A thorough answer depends not only on whether the network operates at 2.4 GHz or below 1 GHz, but also on whether the networked devices are indoors or outside. Other factors include whether they operate at 0 dBm, which is the most common power and which ZigBee chips directly support, or at a higher power. The maximum is 20 dBm, but it requires an amplifier external to the ZigBee chip. The most important variable is how many hops the data makes before reaching its destination.

Although the 2.4-GHz band offers higher data rates than do the 868- and 915-MHz bands, advocates of the less-than-1-GHz frequency, such as ZMD (www.zmd.biz), say that transmission at the lower frequencies is more reliable because fewer users produce interference in the less-than-1-GHz bands and because problems with signal absorption and reflection are less severe at the lower frequencies. Therefore, the lower frequency devices can often operate at lower power.

The ZigBee NWK (network layer) supports star, tree, and mesh topologies (**Figure 4**). Network devices can relay messages from other network devices. In a star topology, a ZigBee coordinator controls the network. The coordinator initiates and maintains the network devices; all other devices are end devices, which directly communicate with the coordinator. In mesh and tree topologies, the coordinator starts the network and chooses certain key network parameters. ZigBee routers can extend the network. In tree networks, routers move data and control messages through the network using a hierarchical- routing strategy. Tree networks can use beacon-oriented communication. Mesh networks allow full peer-to-peer communication.

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Tracking assets during inventory is an interesting application in which ZigBee may be more useful than the technology usually associated with the application: RFID (radio-frequency identification). RFID tags are passive; they receive the energy they use to respond to a query from the RF signal that issues the query. The problem is that the device that sends the query must usually be no more than about 3m from the RFID tag that provides the response. If you are, say, trying to locate test instruments in a large R&D or manufacturing complex, this characteristic presents a Catch-22: It doesn't make much sense to have to know where an item is to find it! A ZigBee network, however, can track the locations of instruments throughout a large campus. Each instrument must have a ZigBee platform, which is more expensive than an RFID tag, but, within the first year, the labor savings during inventory or when the calibration lab must retrieve instruments for calibration might easily exceed the ZigBee platform's cost differential.

TORTOISE OVER HARE

ZigBee's progress in industrial applications probably won't set speed records, but the technology is likely to win the race over competing technologies in the same way that the fabled tortoise triumphed over the hare—slowly and steadily. For example, it will take a good while before ZigBee can demonstrate the "five-nines" (99.999%) uptime that many industrial applications require. A major reason that such demonstrations will take time is the protocol's low speed when users apply it as its developers intend. Transaction-based applications measure ZigBee's speed not in transactions per second but

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in transactions per minute, per hour, or even per month. Moreover, in predicting the reliability of real-world applications, you must deal with statistics and probability. Thus, it can take many months to demonstrate with high confidence that an application is subject to no more than one error per month. In the test community, the speed issue has led some to believe that validation protocols based on bit- or frame-error rates are inappropriate for ZigBee and that tests based on EVM (error-vector magnitude) will more quickly yield accurate answers. Still, the warm initial reception the industry has accorded to ZigBee technology is encouraging Alliance members. Developers downloaded more than 18,000 copies of the ZigBee specification in its first year after publication.

IF LOCATING A ZIGBEE SENSOR IN JUST THE RIGHT SPOT REQUIRED EXTRAORDINARY EFFORT, USERS WOULD LIKELY POSTPONE BATTERY REPLACEMENT UNTIL THE BATTERY DIED AND CAUSED A POSSIBLY EXPENSIVE FAILURE.

Another issue that enters the thinking of prospective ZigBee users in industry is ZigBee devices' dependence on batteries. ZigBee ICs that have the wherewithal to measure the state of charge of the batteries that supply their power and routines for sending alarm messages shortly before batteries need replacement are among those that development-tool suppliers provide for embedding in the ZigBee stack. Nevertheless, if locating a ZigBee sensor in just the right spot required extraordinary effort, users would likely postpone battery replacement until the battery died and caused a possibly expensive failure.

Several techniques for extending battery life or eliminating batteries come to mind. If you can embed more intelligence in the sensor so that it can—without consuming much energy—make data-dependent decisions independently without involving remote system elements, you can reduce the sensor's need to communicate and reduce the need for much of the energy that communication uses. However, such smart sensors present not only a formidable hardware-design problem, but also significant software-design challenges (**Reference 3**).

A different approach involves getting small amounts of energy from the environment through a panoply of techniques known as energy harvesting (**Reference 4**). For example, in a well-lit factory or office, solar cells might power a ZigBee device. A ZigBee light switch might obtain its energy from the movement of the toggle and store it in an ultracapacitor. (Light switches that need no ac connections *do* make sense! They can reduce wiring costs and simplify changes in office layouts.) Perhaps manufacturers can harvest energy from the stray ac magnetic fields surrounding wires that deliver power to motors and office machines. And they can harvest energy from the vibrations of production machinery. EDN

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AUTHOR'S BIOGRAPHY

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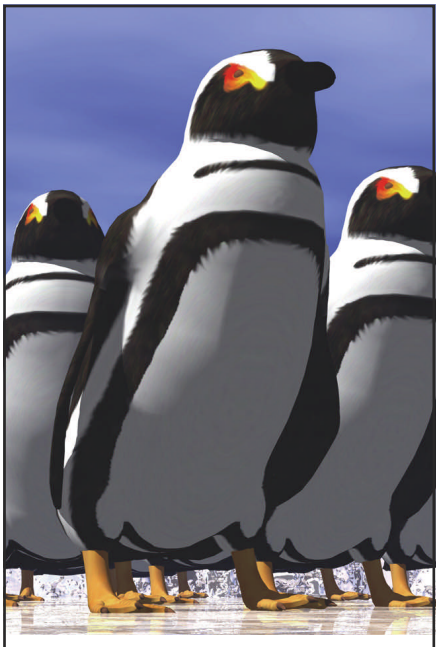

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Power-management techniques for multimedia mobile phones

ASIA AND OTHER MARKETS ARE RACING TO LAUNCH DIGITAL TV AND STREAMING VIDEO AND MUSIC IN HAND-HELD FORMATS. THESE TECHNOLOGIES BRING BENEFITS, BUT DESIGNERS STILL FACE THE CONSTRAINTS OF INCORPORATING MULTIMEDIA FUNCTIONS IN SMALL FORM FACTORS IN THE FACE OF INCREASING BATTERY LIFE.

Now that Asia and other markets race to deploy portable-media technology in the form of multimedia phones, designers must take a step back and consider power-management issues for these handheld devices (see **sidebar** "Asia looks to multimedia as the new 'new thing'"). Consumers have come to expect the small form factor and the long battery life on the 2G and 2.5G GSM (Global System for Mobile communication) or CDMA (code-division multiple-access) phones available today. The challenges to mobile-phone designers now are to include the new multimedia functions and still maintain the small, low-profile form factor of the handsets, as well as their long battery life. No one wants to deploy a handset that users would have to recharge after two hours of operation.

New application processors can deliver the necessary media-processing functions, but it comes at the price of higher power consumption. And the new devices change the users' profiles, as well. New audio and video functions mean longer audio-playback time, so audio amplification needs to be more efficient. Moreover, as audio and video functions on mobile phones mature, competition will increase the standard of audio quality and output power. All of these added power drains must somehow fit into an already-constrained power budget. Designers must tackle these challenges at all levels of system design, and, although the industry has focused on the digital SOCs (systems on chips) that form the hearts of these handsets, the analog portion of the handset can also help solve these design problems.

To achieve a small-phone form factor, designers commonly

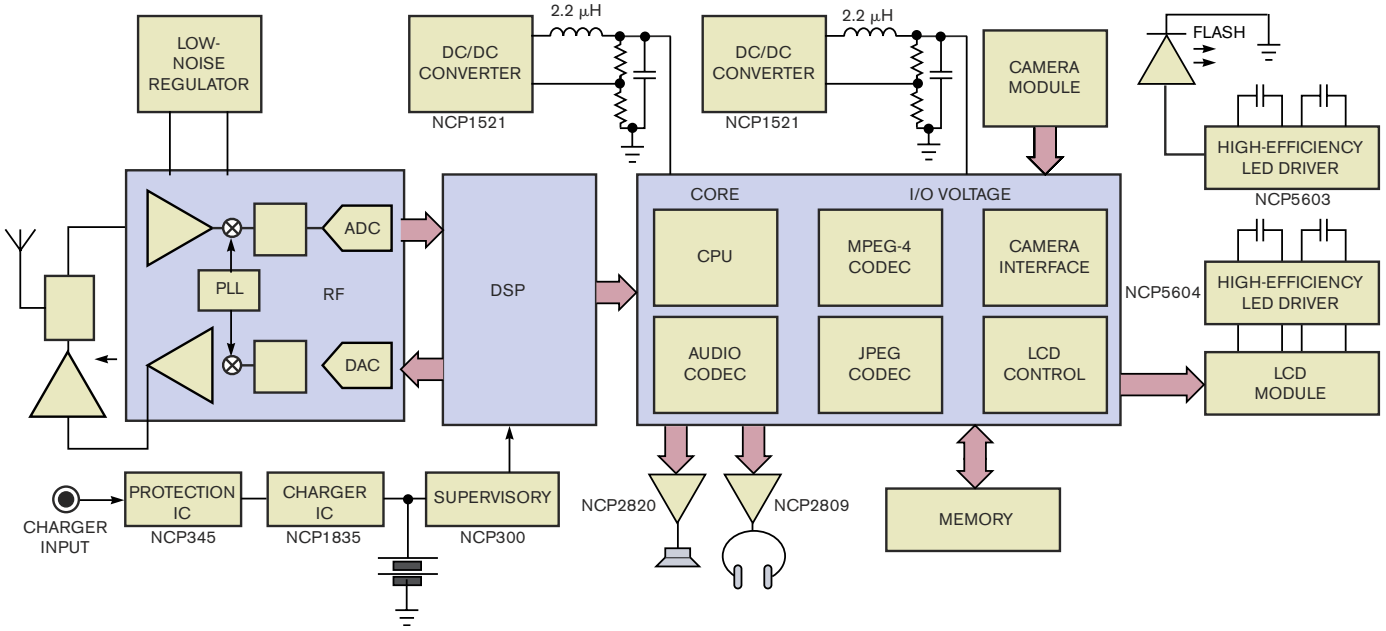

Figure 1 An MPEG-4 platform requires a dc/dc step-down converter with power efficiency greater than 90% and low heat dissipation.

use an integrated power-management unit, which simplifies the power-supply design and makes the end product smaller than it would be if it required the use of several discrete power sections. Paradoxically, however, just as the fast development of multimedia functions in the handsets has increased the need for compactness and power efficiency, it has also led to increased usage of stand-alone voltage regulators. Power-management units are simply too weak to support the increasing power requirements of today's multimedia-rich application processors. And shorter mobile-development-cycle time has not allowed designers to wait for the power-management unit's output power to catch up. As a result, stand-alone voltage regulators supply the extra system power that mobile handsets require.

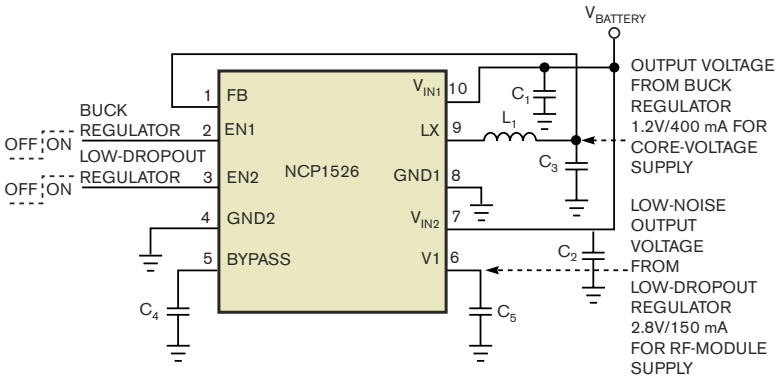

Figure 2 Vendors are beginning to introduce integrated power ICs with both buck and low-noise, low-dropout regulators.

Thus, designers must carefully select stand-alone regulators. Apart from total cost, the top three criteria in the selection of a stand-alone voltage regulator are low noise, low power consumption, and small form factor. The low-dropout regulator is usually a designer's first choice. Low-dropout regulators are simple to design, they generate no significant amount of noise, and they provide fast response. However, to minimize the power loss and heat that are inevitable with linear regulation, experts often recommend low-dropout regulators only in low-power applications or in cases in which the output voltages are close to the input voltages. Lithium-ion cells in typical handset applications have output-voltage ranges of 4.2 to 3V, making the low-dropout regulator suitable to supply the 3.3 or 3V that analog-I/O circuits commonly require. Despite their inefficiency, low-dropout regulators provide clean power to sensitive circuits, such as RF stages.

In contrast, microprocessor-core voltages are constantly decreasing because of smaller process geometries; 1.8, 1.5, and even 1.2V have become common in SOCs. At these voltages, the difference between the input and the output voltage of the regulator becomes too large for the low-dropout regulator to achieve acceptable efficiency. If a low-dropout regulator supplies such low core voltage, the loss in power conversion drastically reduces the battery life, and the increase in heat dissipation within the handset enclosure eventually reduces the product's lifetime.

The ideal voltage regulator for new processors is not the simple, quiet low-dropout regulator, but a dc/dc step-down converter with power efficiency greater than 90% and low heat dissipation (**Figure 1**). An appropriate synchronous step-down converter can supply the core voltage of a low-voltage, deep-submicron chip set, as well as the higher voltage to the I/O circuitry. Buck converters with internal synchronous rectifiers can

ASIA LOOKS TO MULTIMEDIA AS THE NEW "NEW THING"

By Margery Conner, Technical Editor

The Asian market is once again leading the way in innovative mobile-phone applications–this time as go-everywhere multimedia platforms. According to this article's author, Crystal Lam, product-line manager at the Analog Low Power Management Business Unit at On Semiconductor, the new MPEG-4 phones currently popular in Korea and China are the first devices in the coming onslaught of streaming-music and -video phones. "In Asia, portable TV is no longer a dream," she says. The devices allow users to download and play streaming video and MP3 music. In Asia, portable TV is becoming a reality. With the S-DMB (satellite-digital-multimedia-broadcasting) service Korea launched last May, consumers can watch TV programs on their handsets for a monthly subscription fee. China subsequently introduced the service and launched the first digital-TV-broadcast service based on the DMB standard in Shanghai last November. Lam predicts that network operators will subsidize the phone price with the revenues from data transfer and subscriptions, making the new multimedia phones available at an affordable price.

Even traditional content providers are taking a leading role in driving mobile-media-technology development. Seven months after the launch of the S-DMB service, Korean TV channels released a free TV-broadcast service based on the T-DMB (terrestrial-DMB) standard. Despite the reluctance of the network operators to promote the T-DMB phones, Samsung has released seven T-DMB handsets, and LG has presented its T-DMB-enabled PDA with a 3.5-in. LCD screen that can broadcast a TV program during a 2.5-hour window each day. Whichever digital-TV standard prevails, Asian phone manufacturers are all preparing for digital-TV services to enter the market during the next 18 months.

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eliminate the use of some external Schottky diodes and offer efficiency of 90 to 96% in full operation over 0.9 to 3.3V with output current as high as 600 mA. Synchronous PWM converters have their own drawbacks in this application, however: They are inefficient under light loads. In mobile phones, the application microprocessors spend most of their time in standby mode. By decreasing their operating power, the microprocessors put the dc/dc converter into the light-loading zone in which efficiency drops to less than 90%. To reduce power consumption in the long-standby time, designers may want to consider using an alternative power supply that employs PFM (pulse-frequency modulation). In this mode, the switching frequency is proportional to the loading, and the overall efficiency thus remains high. Some converters today can automatically switch between modes depending on the demand.

To reduce power-supply size, vendors have moved up to switching frequencies of 1 to 2 MHz for their buck converters. To demonstrate the effect of the switching frequency, consider three similar converters. A 1-MHz step-down converter uses an optimized inductor-capacitor filter with inductance of 10 µH and output capacitance of 10 µF. In contrast, a similar regulator that switches at 1.5 MHz requires respective output-filter-component values of 2.2 µH and 10 µF. Similarly, with a 3-MHz oscillation frequency, the optimized inductor-capacitor-filter values are 2.2 µH and 4.7 µF, respectively.

This comparison shows that the higher the switching frequency, the smaller the inductor and output capacitor necessary and, thus, the smaller the parts. In multimedia-mobile design with tight pc-board constraints, you should use converters with higher switching frequency to minimize the size and reduce the cost of the passive components. The 3×3-mm SOT23-5 industry-standard package is the common choice for synchronous step-down converters. However, smaller package options, such as chip-scale and DFN packages, are also available to meet even tighter size requirements.

A dc/dc buck converter is the best choice for powering application processors. On the other hand, low-noise, low-dropout regulators typically power RF-sensitive analog circuits with input voltages of 2.8 to 3.3V. Ultimately, only further integration can significantly reduce board area in these designs. Accordingly, vendors are beginning to introduce integrated power ICs with both buck and low-noise, low-dropout regulators (**Figure 2**).

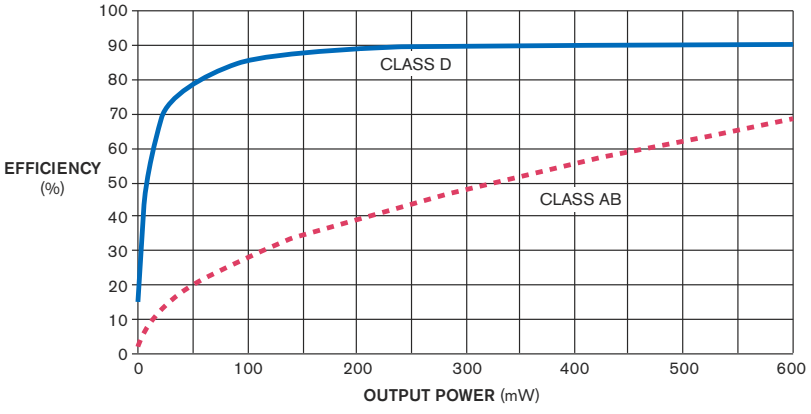

Figure 3 Class D amplifiers offer a stable 85 to 90% efficiency, but the efficiency of Class AB remains 30 to 60%.

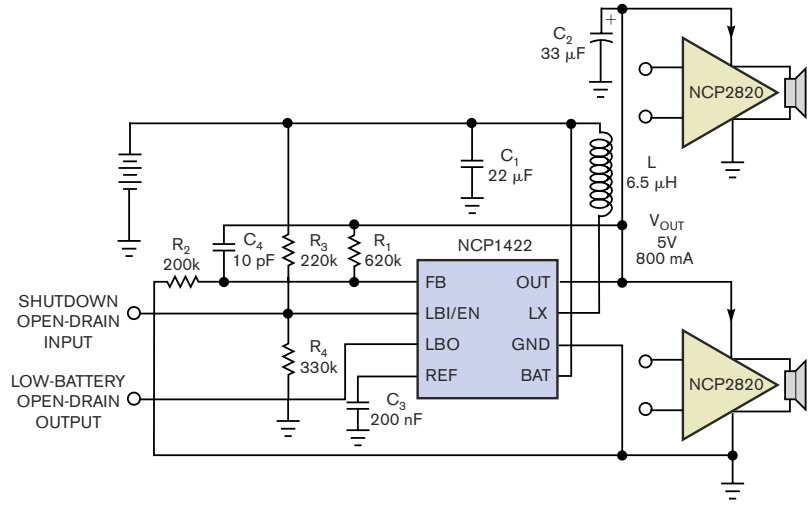

Figure 4 A dc/dc boost converter provides a constant 5V to power the two Class D amplifiers that a stereo application requires.

AUDIO-PLAYBACK CHALLENGES

Portable multimedia functions pose two challenges to audio amplification in mobile phones. First, multimedia phones need to allow continuous music and video playback for at least two hours; long audio-playback time is a key selection criterion on multimedia phones. Second, audio experience on mobile devices must approach that of a home audio system. Users expect clean, powerful stereo audio with bass-boost playback. Today, mobile phones use Class AB audio amplifiers. A typical Class AB audio amplifier offers high audio quality with typical THD+N (total harmonic distortion plus noise) of less than 0.1%. These amplifiers also have good power-supply-rejection ratios, and, thanks to the linear nature of Class AB amplifiers, they present no risk of interfering with the RF system on board. Although they have low power efficiency, they find wide use in short-duration, low-power-audio applications, such as hands-free speakers for voice and ring-tone playback.

But, as MP3 becomes a popular application on mobile-media platforms and playback

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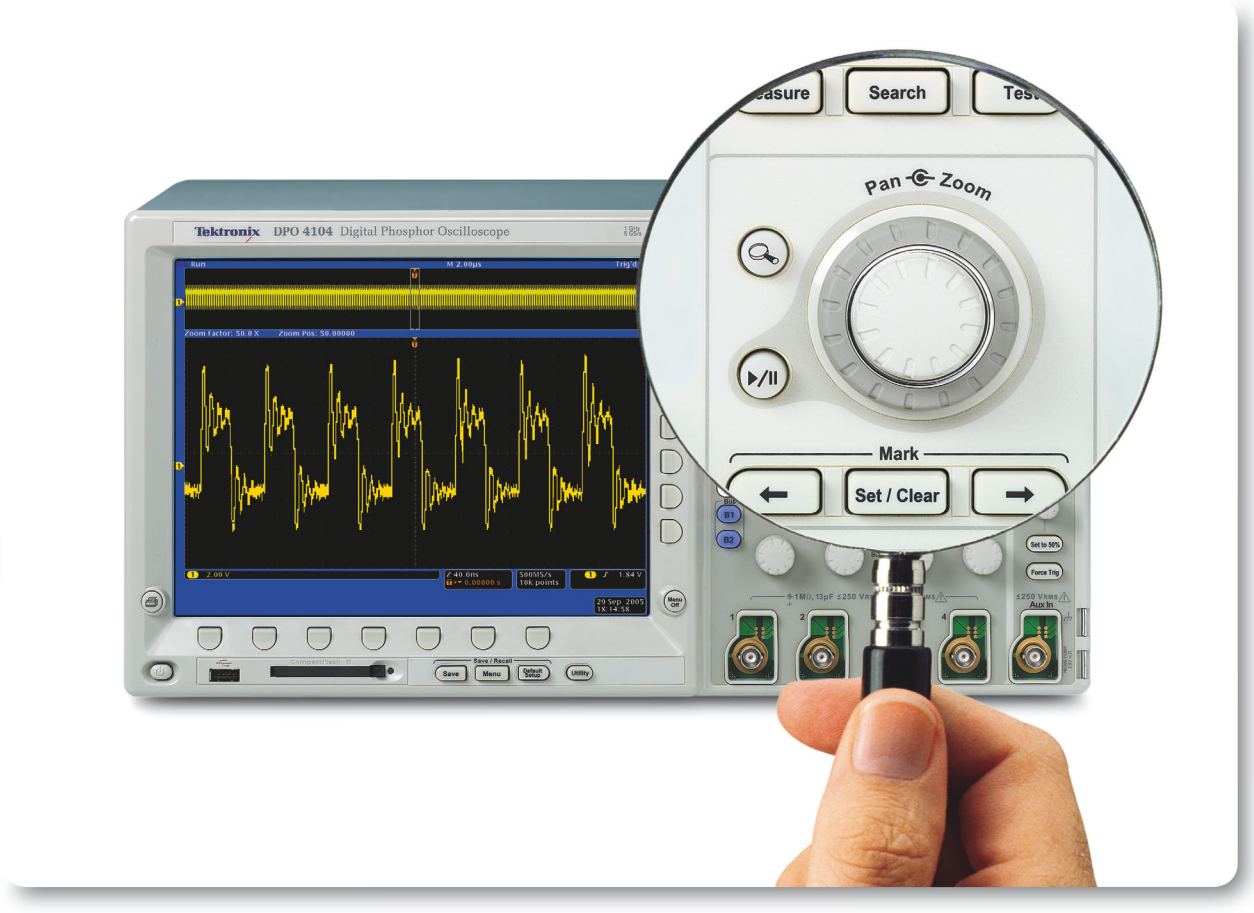

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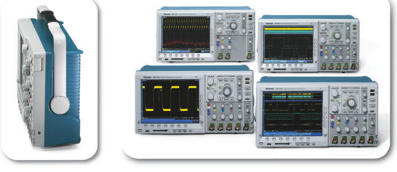

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time increases from a few minutes to hours, Class AB's low efficiency and high heat output will no longer meet the challenge. New designs are now instead employing Class D audio amplifiers. Nominal power consumption for audio amplification in midrange phones is less than 100 mW, and maximum output power is 700 mW. Comparing the efficiency of a typical Class AB and a selected Class D audio amplifier shows that, at 50 mW, the Class D amp has an efficiency of 80%, whereas the Class AB offers a mere 20%. For the higher power operating range of 100 to 500 mW, Class D amplifiers offer a stable 85 to 90% efficiency, but the efficiency of Class AB remains 30 to 60% (**Figure 3**).

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Due to their low efficiency and hence high heat generation, Class AB amplifiers in these applications cannot be robust enough to deliver output power higher than 1W without saturation or distortion. Thanks to the switching-mode operation in Class D amplifiers, they efficiently amplify the audio signal and thus can deliver higher output power to support high-volume audio playback. You can achieve as much as 1.4W output to an 8Ω speaker at a THD+N of less than 1%. Because low-frequency sound generation requires considerable power, especially with small speaker areas, this extra amplifier power helps to boost the bass sound, which is an important feature in music and gaming audio playback.

MP3 players—and, most likely, future mobile-media devices—often use an external cradle with 4Ω stereo speakers. This requirement provides another challenge to the audio amplifier, which you can best meet by operating the device at a higher voltage, such as 5 to 5.5V. This approach, in turn, requires a dc/dc boost converter to provide a constant 5V to power the two Class D amplifiers that a stereo application requires (**Figure 4**).

EMI CONSIDERATIONS

A Class D amplifier operates in a constant-frequency PWM-switching mode. Thus, it may produce EMI that can interfere with nearby RF-circuit operation. Two key techniques can help prevent EMI interference with the RF system. First, you should place the Class D amplifier close to the speaker. In the case of stereo applications, you should use two monophonic amplifiers rather than a single stereo chip, so that you can place the two amplifiers next to the two speakers, usually at the sides of the handset. Apart from this step, designers should also connect an EMI filter, such as a ferrite bead, to the output of the amplifier. The EMI filter acts as a bandpass filter to remove the high-frequency switching signal from the audio output before it can propagate along the traces to the RF circuitry.

Market forces are driving mobile-multimedia devices to replace mobile phones in both mature and developing markets. In these new mobile-media centers, vendors are upgrading processors and releasing chip sets at such a pace that integrated-power approaches from the power vendors can't keep up. Thus, designers of the new mobile-media centers must turn to discrete power and audio devices to meet the extra system requirements and to deliver new models with short time to market.

VENDORS ARE UPGRADING PROCESSORS AND RELEASING CHIP SETS AT SUCH A PACE THAT INTEGRATED-POWER APPROACHES FROM THE POWER VENDORS CAN'T KEEP UP.

New synchronous buck converters offer high efficiency, are easy to design-in, and help designers to develop small systems with low system cost. Similarly, Class D audio amplifiers with high power efficiency prolong audio-playback time to meet new market demand. Class D amplifiers also deliver high output power to support the compelling audio playback critical in MP3, TV, and gaming functions. EDN

AUTHOR'S BIOGRAPHY

Crystal Lam is a product-line manager for ON Semiconductor's analog low-voltage power-management products in the company's Toulouse, France, development center.

Ultrafast Fixed Gain Amplifiers Simplify High Resolution Video Designs

High Performance Analog Solutions from Linear Technology

Whether using composite, S-Video or component video, systems require high performance amplifiers for driving cables, adding gain, converting between formats and shaping the video signals. The increased dimensions of high-definition LCD displays require amplifiers with high gain bandwidth and slew rate to scan the entire screen in one refresh cycle. Low supply voltages present special challenges in video designs, forcing amplifiers to accommodate the video signal's relatively large swings and high slew rates within limited supply rails.

UXGA Resolution

The proliferation of high-resolution video displays, both in the professional and consumer markets, has markedly increased the analog bandwidth of baseband video signals. For example, digital studio equipment for NTSC broadcast television typically uses pixel rates around 14 million per second, while now ubiquitous XGA computer outputs (1024 x 768) routinely churn out about 80Mpixels per second. The latest high definition consumer formats put out a comparable 75Mpixel per second stream and the increasingly popular UXGA professional graphics format (1600 x 1200) generates a whopping 200Mpixels per second flow. Accurate video reproduction of these newer formats is placing exceptional demands on the frequency response of video amplifiers. Specifically, pulse-amplitude waveforms like those of baseband video require reproduction of high-frequency content up to at least the 5th harmonic of the fundamental frequency component. This is 2.5 times the video pixel rate, accounting for 2 pixels per fundamental cycle relationship, indicating that UXGA pushes flat frequency response beyond 500MHz.

Baseband video generated at these higher rates is processed in either native red-green-blue (RGB) domain or encoded into "component" luma plus blue-red chroma channels (YPbPr); three channels of information in either case. With frequency response requirements extending beyond 500MHz, amplifier layouts

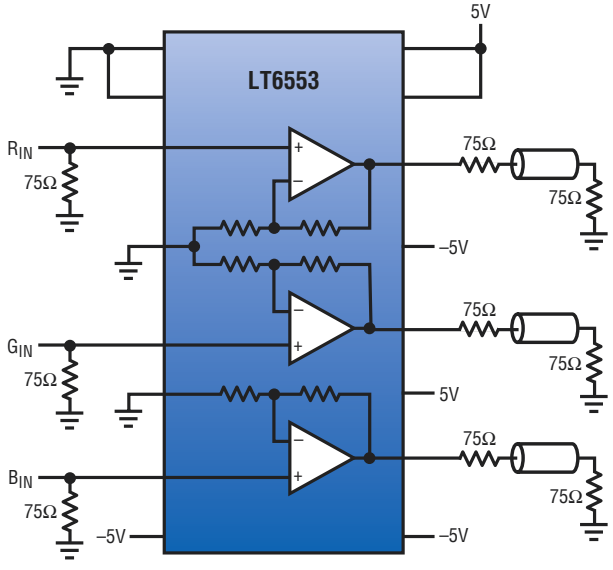

Figure 1. LT6553 RGB Cable Driver Circuit

Ultrafast Fixed Gain Amplifiers Simplify High Resolution Video Designs

that require external resistors for gain setting tend to waste valuable real-estate. Furthermore, frequency response and crosstalk anomalies can plague the printed circuit development process.

The LT®6553 and LT6554 triple amplifiers solve these problems, providing internal factory matched resistors and an efficient 3-channel flow-through layout arrangement using a compact 16-pin SSOP package. They offer 650MHz bandwidth with an ultra-high slew rate of 2500V/us. The 0.1% settling time is a quick 6ns for a 2V step. This makes them ideal for RGB video processing on displays with UXGA resolution (1600 x 1200 pixels). The LT6553 has an internal fixed gain of two and is intended for driving 50Ω or 75Ω back-terminated cables (for effective loading of 100Ω and 150Ω respectively). The LT6554 is internally configured for unity gain, making it useful for driving ADCs or other high impedance loads characterized with 1kΩ as a reference loading condition. Figure 1 shows the typical RGB cable driver application of an LT6553. Its excellent time response characteristics are shown in Figure 2. The amplifiers's frequency response exhibits only –0.5dB attenuation at 450MHz, with minimal peaking.

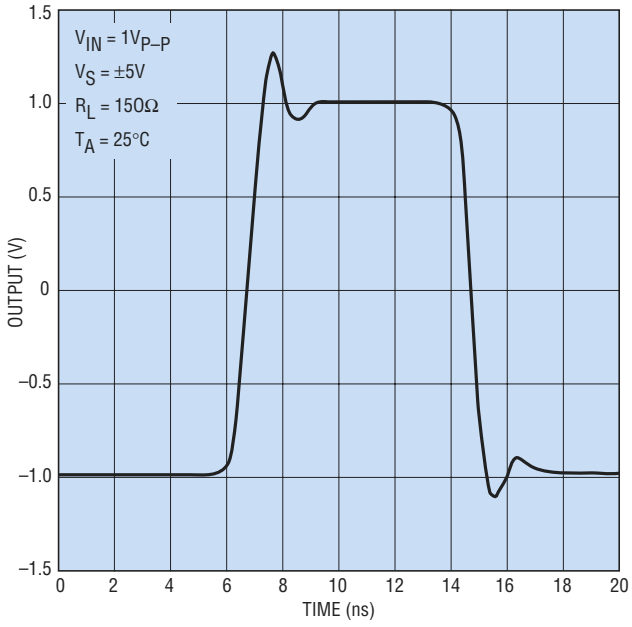

Figure 2. Fast Pulse Response

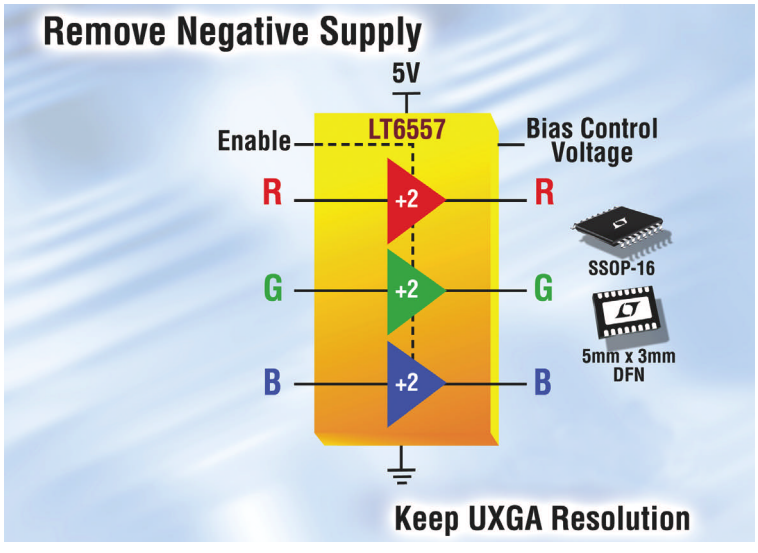

Figure 3. LT6557 Single Supply RGB Amplifier

Operating with the Right Power Supplies

The LT6553 and LT6554 require a total power supply of at least 4.5V, but depending on the input and output swings required, may need more to avoid clipping the signal. The LT6554 has unity gain, making the analysis simple. The output swing is about (V^+ - V^-) – 2.5V and is only governed by the output saturation voltages. This means a total supply of 5V is adequate for standard video ($1V_{P-P}$). For the LT6553, extra allowance is required for load driving, so the output swing is (V^+ - V^-) – 3.8V. This means a total supply of about 6V is required for the output to swing $2V_{P-P}$, as when driving cables. For best dynamic range along with reasonable power consumption, a good choice of supplies would be ±3V or the LT6554 and 5V/-3V for the LT6553. Since many systems today lack a negative supply rail, the new LT6557 triple video amplifier offers an excellent solution with its true single supply capability.

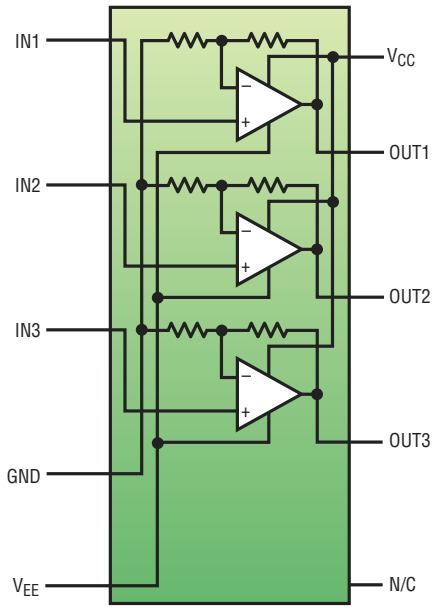

Figure 4a. LT6550 Block Diagram

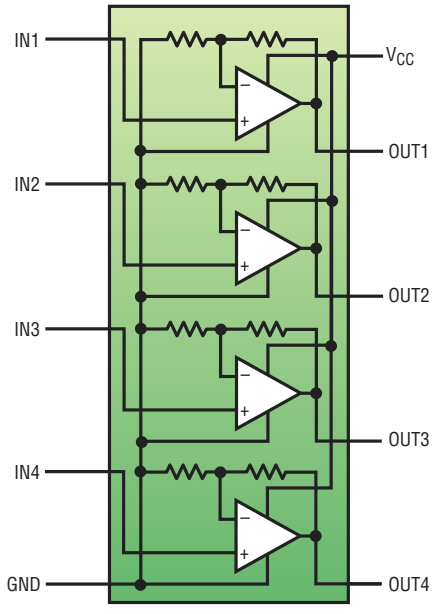

Figure 4b. LT6551 Block Diagram

Handling AC-Coupled Video Signals

AC-coupled video inputs are more difficult to handle than those with DC-coupling because the average signal voltage of the video waveform is affected by the picture content, such that the black level at the amplifier wanders with scene brightness. In NTSC and PAL video systems, 700mV is the approximate difference between the maximum signal voltage and black level. When a video signal is AC-coupled, the amount of dynamic range required to handle the signal is potentially double that required for DC-coupled operation. This represents a challenge, especially for video systems operating from a single 5V supply. The LT6557 RGB amplifier solves this problem by featuring a wide output swing that extends to 0.8V of supply rails. On a 5V single supply, it achieves 3.4V of dynamic range, which is adequate for standard video.

The LT6557 uses a unique internal architecture that simplifies the task of implementing high-speed video signals in single supply applications. An internal biasing feature allows the user to program the inputs of all three amplifiers with a single resistor to a desired DC bias voltage level. This feature minimizes external component count and provides ease of use in AC-coupled applications. Furthermore, the internal fixed gain of 2 eliminates six external gain-setting resistors required for driving double terminated cables. The LT6557 is the fastest RGB amplifier on the market capable of providing full video swing when operated from a 5V single supply. Its -3dB bandwidth of 500MHz, fast slew rate of 2200V/µs, coupled with a quick 4ns settling time, enhances AC performance of the amplifier, resulting in sharper video images. In addition, the LT6557 has a 0.1dB gain flatness that extends to 120MHz, facilitating use over a wide range of video signals.

Shrinking Supply Rails

The industry trend toward lower supply voltages increases the demands placed on analog signal handling characteristics. For example, a 3.3V video amplifier not only requires high slew rate and fast settling time, but must also have wide input and output voltage swing ranges to avoid clipping any portion of the video waveform. Current feedback amplifiers cannot be used because they lack sufficient signal swing at low supplies and they require input signals above ground.

The LT6550 and LT6551 are true voltage feedback amplifiers featuring 110MHz (-3dB) bandwidth, 340V/µs slew rate, and fast settling time, making them ideal for low voltage, high resolution RGB video processing. The LT6550 and LT6551 operate from 3V to 12.6V and are fully specified on single 3.3V and 5V supplies. The LT6550 is also specified on ±5V supplies. Both parts are available in compact 10-PIN MSOP packages, enabling compact solutions for driving RGB and component video cables. These voltage feedback amplifiers drive either 50Ω or 75Ω double terminated cables and are preconfigured for a fixed gain of two, eliminating six or eight external gain setting resistors. The block diagrams in Figure 4 show the differences between the LT6550 and LT6551. The LT6551 quad is designed for single supply operation with the feedback returned to ground. The LT6550 triple has a separate VEE pin and can be used on either single or split supplies.

RGB Video Multiplexing

Video multiplexers are required for high speed pixel switching, video signal routing and RGB switching. RGB and YPbPr video signals are commonly multiplexed to reduce I/O connector count or otherwise reuse

Ultrafast Fixed Gain Amplifiers Simplify High Resolution Video Designs

various high-value video signal processing sections when selecting various modes of operation in the end use of the product. This has often been accomplished with the use of FET switches and buffer amps to route the various video channel signals. The LT6555 and LT6556 RGB video multiplexers accomplish this task without the need for external switches.

Featuring resolution beyond UXGA, the LT6555 and LT6556 have a wide bandwidth of 650MHz and a very high slew rate of 2200V/us, enabling them to process large input signals. The LT6555 integrates three 2:1 input multiplexers followed by fixed gain of 2 amplifiers for driving double terminated cables. The LT6556 follows the same topology except the amplifiers have unity gain for buffering or driving ADCs and high impedance loads. In applications with more than two inputs per channel, multiple LT6555s or LT6556s can be connected using the output disable pin to implement larger arrays as shown in Figure 6.

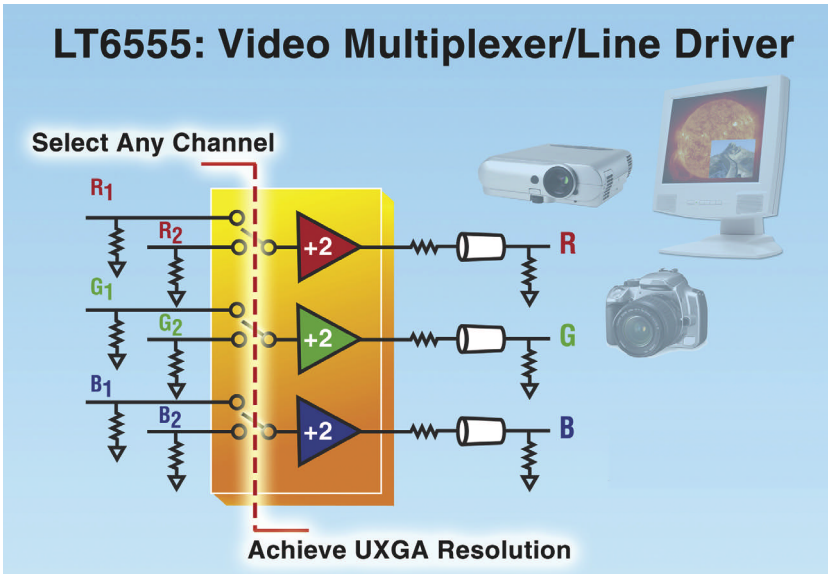

Figure 5. LT6555: Video Multiplexer/Line Driver

Independent supply pins for each amplifier boost channel separation, ensuring excellent crosstalk specifications. This eliminates channel interaction in RGB muxing applications. The devices are capable of operation on dual or single supplies from 4.5V to 12V total. Housed in the space saving 4mm x 4mm QFN and 24-pin SSOP packages, they offer a compact and easy to use solution in a wide variety of video switching applications.

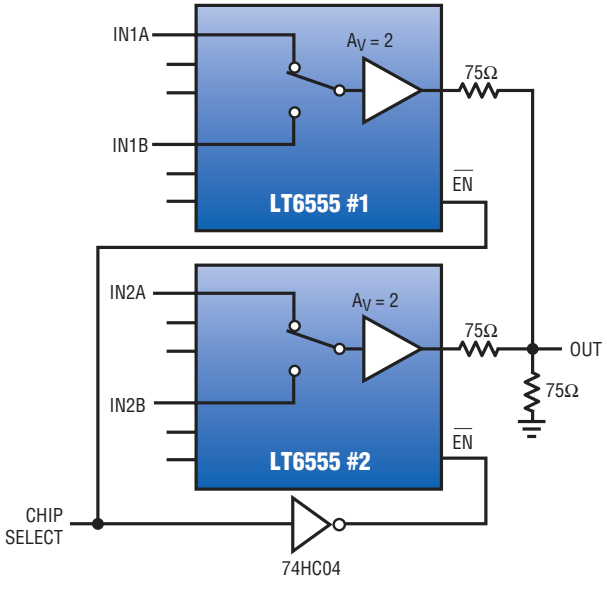

Figure 6. Two LT6555s Build a 4-Input Router

Conclusion

As video resolution increases, system designers require analog components that achieve higher performance than ever before. The challenge is compounded by the desire to reduce board space and to shrink or eliminate system power rails. Linear Technology's latest video products provide high bandwidth, fast slew rate and fast settling time amplifiers, integrated multiplexers and the capability of running on a single supply.

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LINEAR TECHNOLOGY

BY KEN YANG • MAXIM INTEGRATED PRODUCTS

Flatten DAC frequency response

EQUALIZING TECHNIQUES CAN COPE WITH THE NONFLAT FREQUENCY RESPONSE OF A DAC.

In a generic example, a DAC samples a digital baseband signal (**Figure 1**). The DAC's frequency response is not flat; it attenuates the analog output at higher frequencies. At 80% of $f_{NYQUIST}$, for instance ($f_{NYQUIST}=f_S/2$), the frequency response attenuates by 2.42 dB. That amount of loss is unacceptable for some broadband applications requiring a flat frequency response. Fortunately, however, several techniques can cope with the nonflat frequency response of a DAC. These techniques include increasing the DAC's update rate using interpolation techniques, pre-equalization filtering, and post-equalization filtering, all of which reduce or eliminate the effects of the sinc roll-off.

FREQUENCY RESPONSE

To understand the nonflat frequency response of a DAC, consider the DAC input as a train of impulses in the time domain and a corresponding spectrum in the frequency domain (**Figure 2**). An actual DAC output is a "zero-order hold" that holds the voltage constant for an update period of $1/f_S$. In the frequency domain, this zero-order hold introduces sin(x)/x, or aperture, distortion (**Reference 1**). The amplitude of the output-signal spectrum multiplies by sin(x)/x (the sinc envelope), where $x=\pi f/f_S$, and

$$H(f) = \text{sinc}\left(\frac{\pi f}{f_s}\right) = \frac{\sin\left(\frac{\pi f}{f_s}\right)}{\left(\frac{\pi f}{f_s}\right)} \qquad (1)$$

describes the resulting frequency response (**Figure 3**). Thus, aperture distortion acts as a lowpass filter that attenuates image frequencies but also attenuates the desired in-band signals.

The sin(x)/x (sinc) function is well-known in digital-signal processing. For DACs, the input is an impulse, and the output is a constant-voltage pulse with an update period of $1/f_S$ (the impulse response), whose amplitude changes abruptly in response to the next impulse at the input. You obtain the DAC's frequency response by taking the Fourier transform of the impulse response (a voltage pulse, **Reference 2**).

The desired signal frequency in the first Nyquist zone reflects as a mirror image into the second Nyquist zone between $f_S/2$ and f_S, but the sinc function attenuates its amplitude. Image signals also appear in higher Nyquist zones. In general, a lowpass or bandpass filter, often called a reconstruction filter, must remove or attenuate these image frequencies. Such filters are analogous to the antialiasing filter that an ADC often requires.

As the DAC output frequency approaches its update frequency, f_S, the frequency response approaches zero or null. The DAC's output attenuation therefore depends on its update rate. The 0.1-dB-frequency flatness is about $0.17f_{NYQUIST}$, where $f_{NYQUIST}=f_S/2$. As the output frequency approaches $f_S/2$, so does the first image frequency. As a result, the maximum usable DAC output frequency for systems in which filtering removes the image frequency is about 80% of $f_{NYQUIST}$.

The first image frequency is $f_{IMAGE}=f_S-f_{OUT}$. At $f_{OUT}=0.8f_{NYQUIST}$, $f_{IMAGE}=1.2f_{NYQUIST}$, leaving only $0.4f_{NYQUIST}$ between frequency tones for the filter to remove the image. Output frequencies higher than 80% of $f_{NYQUIST}$ make it difficult for a filter to remove the images, but the reduction in usable frequency output allows for realizable reconstruction-filter designs.

SPEED THE UPDATE RATE OR INTERPOLATE?

At 80% of $f_{NYQUIST}$, the output amplitude attenuates by 2.42 dB. For broadband applications requiring a flat frequency response, that amount of attenuation is unacceptable. Because the DAC's output attenuation depends on its update rate, you can minimize the effect of sinc roll-off and push the 0.1-dB flatness to a higher frequency simply by increasing the converter's update rate and keeping the input-signal bandwidth unchanged.

Increasing the DAC's update rate not only reduces the effect of the nonflat frequency response, but also lowers the quantization noise floor and loosens requirements for the reconstruction filter. Drawbacks include a higher cost for the DAC, high-

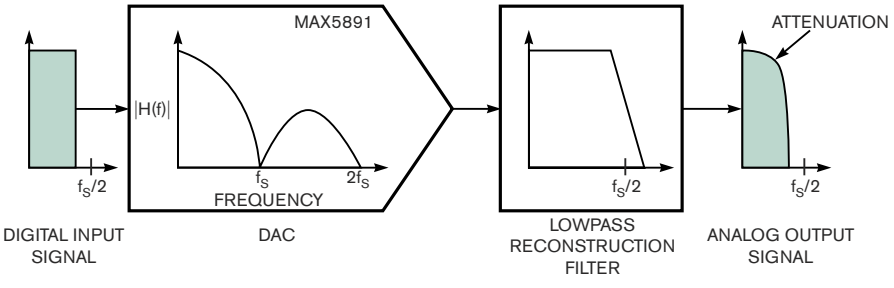

Figure 1 The nonflat frequency response of a DAC attenuates the output signal, especially at high frequencies.

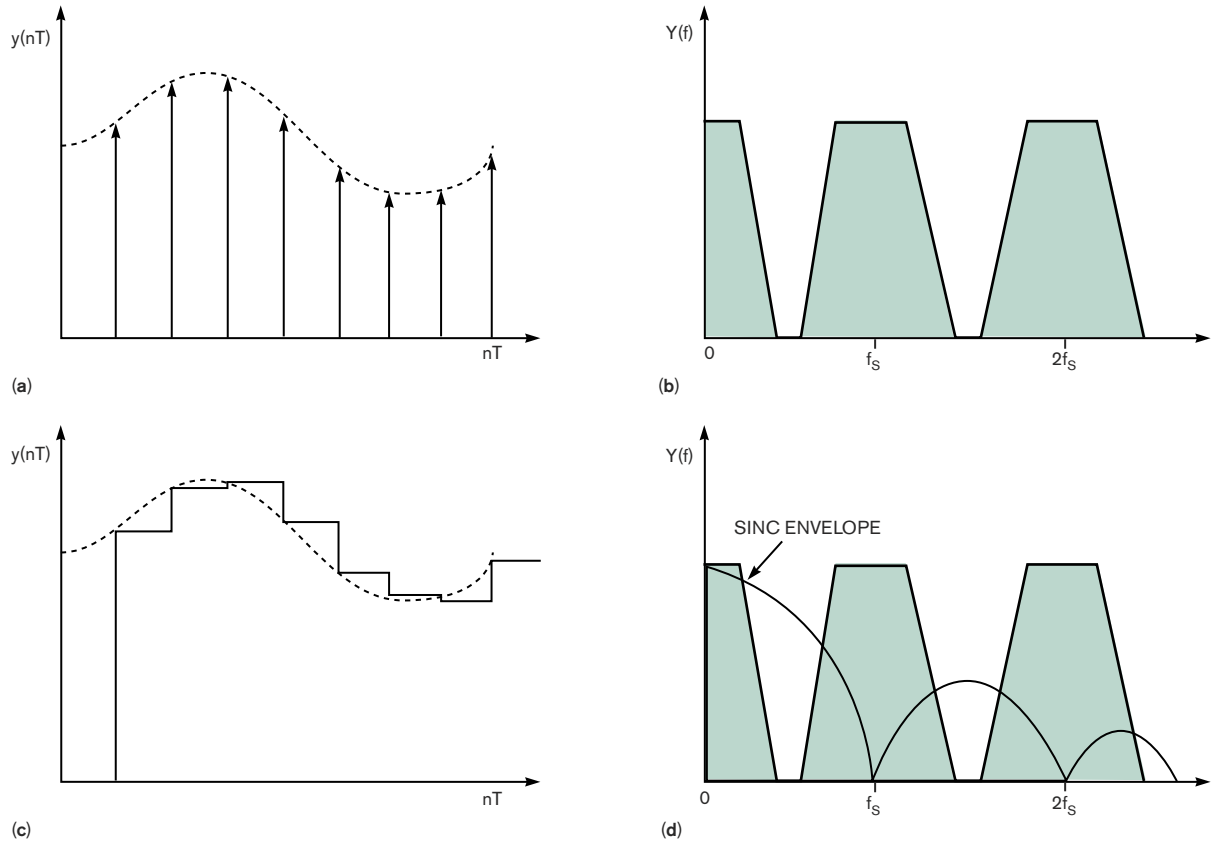

Figure 2 The ideal output from a DAC is a train of voltage impulses in the time domain (a) and a series of image spectra in the frequency domain (b). Actual DACs use a zero-order hold to delay the output voltage for one update period (c), which causes output-signal attenuation by the sinc envelope (d).

er power consumption, and the need for faster data processing. The benefits of higher update rates are so important, however, that manufacturers are introducing interpolation techniques. Interpolating DACs offer all the benefits of higher update rates and keep the input data rate at a lower frequency.

Interpolation DACs include one or more digital filters that insert a sample after each data sample. In the time domain, the interpolator stuffs an extra data sample for every data sample entered, with a value interpolated between each pair of consecutive data-sample values. The total number of data samples increases by a factor of two, so the DAC must update twice as fast.

One modern DAC, for example, incorporates three interpolation stages to achieve an 8× interpolation; the DAC's update rate is eight times the data rate (**Reference 3**). In the frequency domain, the sinc-frequency response also moves out by a factor of eight, as does the effective image frequency, which loosens requirements for the reconstruction filter.

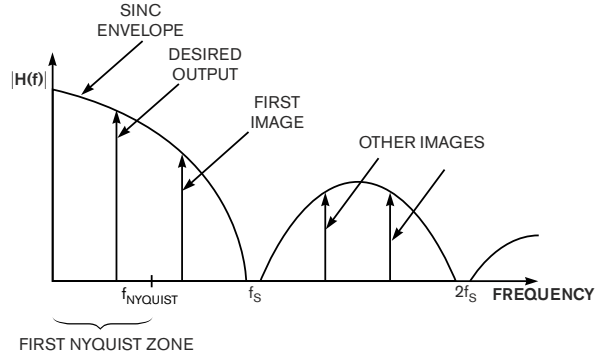

Figure 3 The representation of a DAC output in the frequency domain shows that the desired signal is generally within the first Nyquist zone, but many image signals are present at higher frequencies.

PRE-EQUALIZE?

Increasing the update rate reduces but does not eliminate the effect of sinc-frequency roll-off. If you are already using the fastest DAC available, you must choose other techniques to make additional improvements. It is possible, for example, to design a digital filter whose frequency response is the inverse of the sinc function, that is, 1/sinc(x). In theory, such a pre-equalization filter exactly cancels the effect of the sinc-frequency response, producing a perfectly flat overall frequency response. A pre-equalization filter filters the digital input data to equalize the baseband signal before it sends the data to the DAC. Removing all image frequencies at the DAC output allows original signal reconstruction without attenuation (**Figure 4**).

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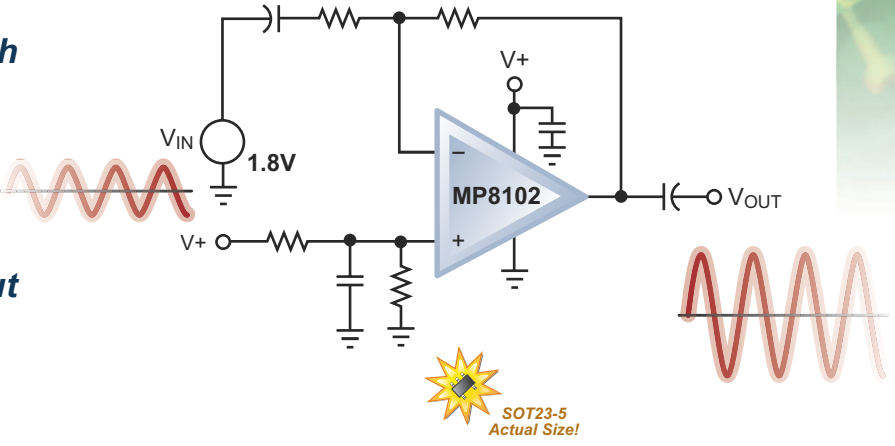

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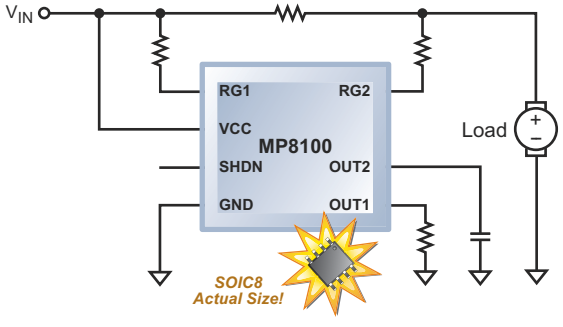

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Any digital filter whose frequency response is the inverse of the sinc function will equalize the DAC's inherent sinc-frequency response. Because the sinc-frequency response is arbitrary, however, a FIR (finite-impulse-response) digital filter is preferable. Frequency-sampling techniques are useful in designing the FIR filter. Assuming the signal is in the first Nyquist zone, you sample the frequency response, H(f), from dc to $0.5f_S$ (**Figure 5**). Then, using the inverse-Fourier transform, you transform the frequency sample points, H(k), to impulse responses in the time domain. The impulse response coefficients are:

$$h(n) = \frac{1}{N}\sum_{k=0}^{N-1} H(k)e^{j(2\pi/N)nk} \quad (2)$$

and

$$h(n) = \frac{1}{N}\left[\sum_{k=1}^{N/2-1} 2|H(k)|\cos(2\pi k(n-\alpha)/N) + H(0)\right], \quad (3)$$

where H(k) and k=0, 1, ... N−1 represent the ideal or targeted frequency response. The quantities h(n) and n=0, 1, ... N−1 are the impulse responses of H(k) in the time domain, and $\alpha=(N-1)/2$. For a linear-phase FIR filter with positive symmetry and even N, you can simplify h(n) using **Equation 3**. For odd N, the upper limit in the summation is (N−1)/2 (**Reference 1**).

Increasing the number of frequency sample points (N) of H(k) produces a frequency response closer to the targeted response. A filter with too few sample points reduces the effectiveness of the equalizer by producing a larger deviation from the target frequency response. On the other hand, a filter with too many sample points requires more digital-processing power. A good technique uses large N for computing h(n), truncates h(n) to a small number of points, and then applies a window to smooth h(n) and produce an accurate frequency response.

A sample filter uses N=800 to compute h(n) (**Figure 6**). You then truncate h(n) to only 100 points and apply a Blackman window to h(n). The frequency response for the combined FIR filter and DAC sinc response exhibits 0.1-dB flatness nearly up to the Nyquist frequency (to approximately 96% of $f_{NYQUIST}$, where $f_{NYQUIST}=f_S/2$). In contrast, the uncompensated DAC response maintains 0.1-dB flatness only to 17% of $f_{NYQUIST}$. Because the filter gain is greater than unity, you must take care that the filter's output amplitude does not exceed the DAC's maximum allowed input level.

After obtaining the impulse-response coefficients, you can implement the FIR filter using a standard digital-processing technique. That is, h(n) filters the input signal data x(n):

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k). \quad (4)$$

Dynamic performance for the compensated DAC is lower than that of the uncompensated DAC, because higher gain at the higher input frequencies requires that you intentionally lower the signal level to avoid clipping the input. Assuming the input is a single tone between dc and f_{MAX} (less than $f_S/2$), the attenuation depends on f_{MAX}:

$$V_{IC} = \frac{\sin\left(\pi f_{MAX}/f_s\right)}{\pi f_{MAX}/f_s} V_{REF}, \quad (5)$$

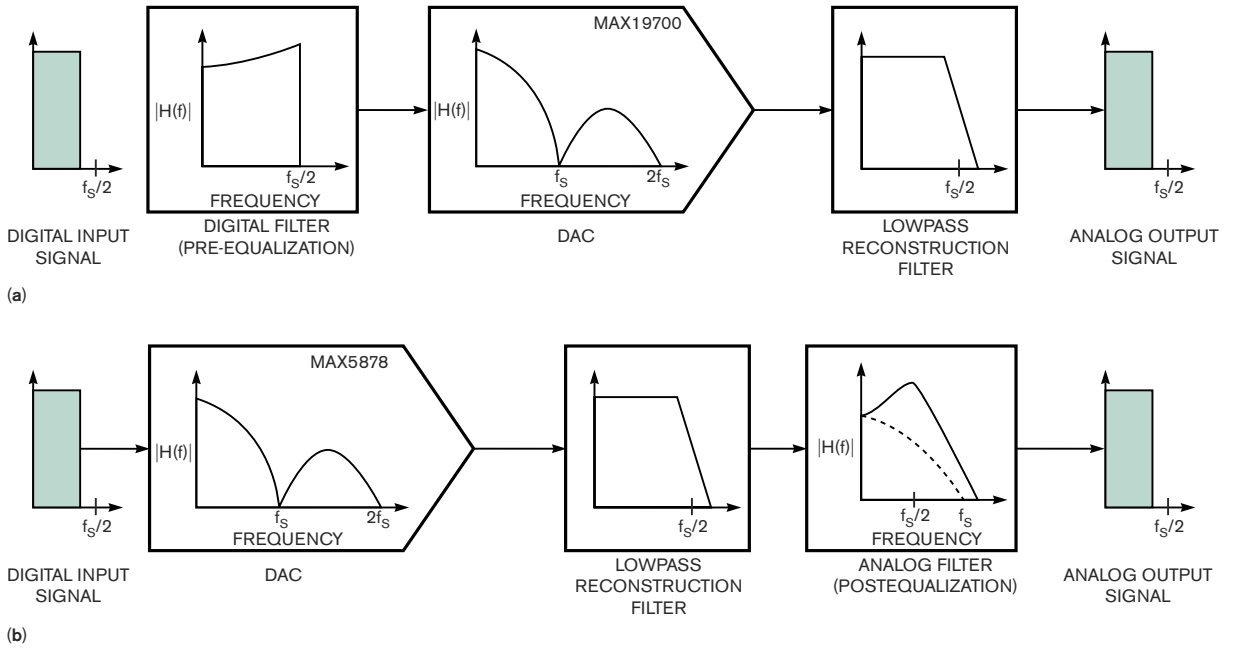

Figure 4 A pre-equalization digital filter cancels the effect of sinc roll-off in a DAC (a). As an alternative, you can use a postequalization analog filter for the same purpose (b).

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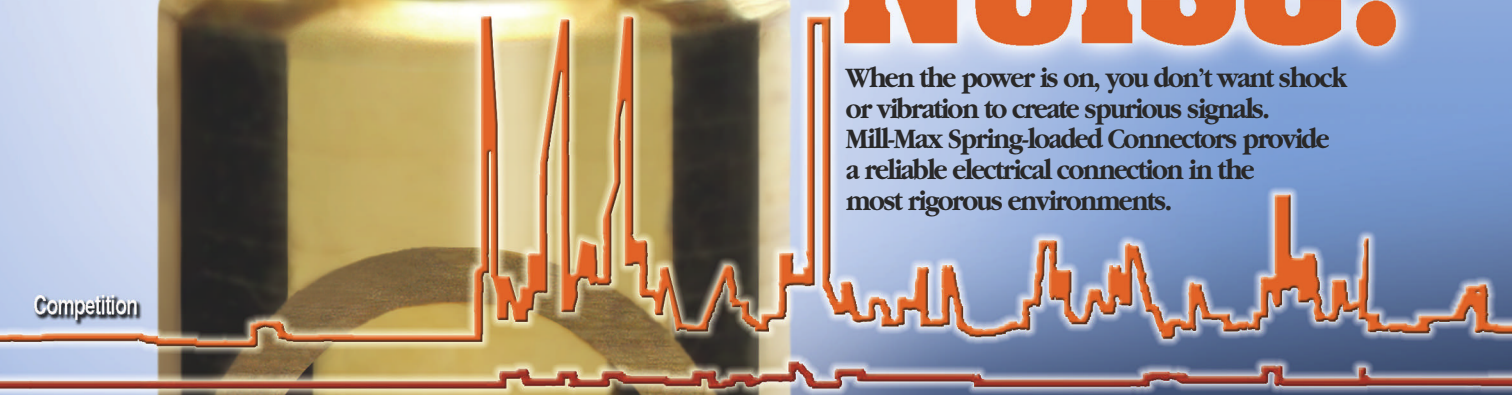

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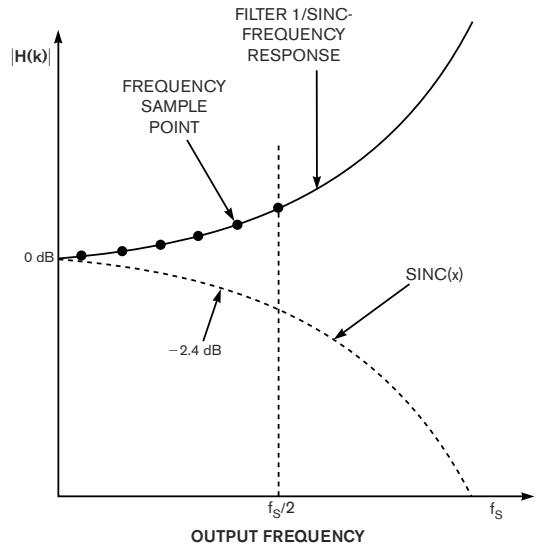

Figure 5 You design a digital pre-equalization filter by sampling the inverse sinc-frequency response from dc to $f_S/2$.

where V_{IC} is the input voltage for the compensated DAC, and V_{REF} is the reference voltage. If, for example, the maximum anticipated input frequency is $f_{MAX}=0.8f_{NYQUIST}$, you must attenuate the DAC input by $V_{IC}=-2.4$ dB below V_{REF}.

The resulting output amplitude is flat over frequency, representing perfect compensation, and equals the input amplitude of $V_{OC}=V_{IC}=-2.4$ dB below V_{REF}. You obtain output noise by integrating the noise power density from near dc to the reconstruction filter's cutoff frequency. DAC manufacturers also often specify SNR by integrating the noise out to $f_{NYQUIST}$ without the use of a reconstruction filter:

$$N_C = \int_0^{f_{NYQUIST}} n_Q(f)df, \quad (6)$$

where N_C is the total noise power or voltage of the compensated DAC, and $n_Q(f)$ is the DAC's output noise density, which

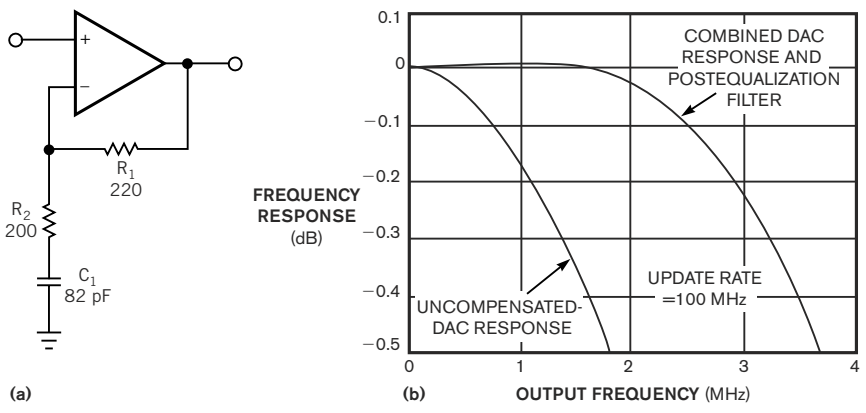

Figure 7 A simple active analog equalizer (a), which you can use to reduce the effects of DAC sinc roll-off, increases the 0.1-dB flatness from 17 to 50% of $f_{NYQUIST}$ (b).

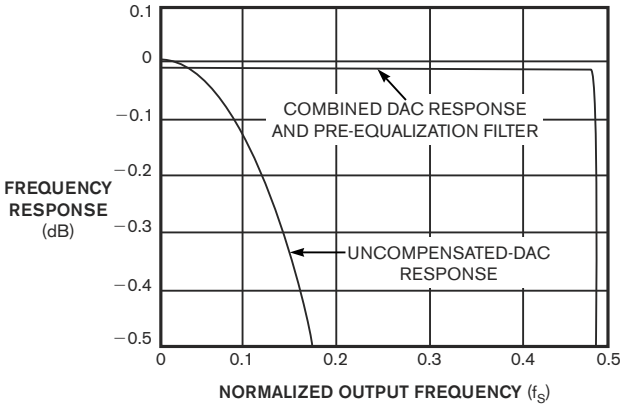

Figure 6 The FIR filter equalizes the DAC's sinc response and achieves 0.1-dB flatness up to 96% of $f_{NYQUIST}$.

is usually limited by quantization noise and thermal noise. The maximum SNR for the compensated DAC is constant and independent of frequency, but it depends on the maximum anticipated output frequency:

$$SNR_C = \frac{V_{OC}}{N_C} = \frac{\sin\left(\pi f_{MAX}/f_s\right)}{\pi f_{MAX}/f_s}\frac{V_{REF}}{N_C}, \quad (7)$$

where V_{OC} is the output amplitude. For the uncompensated DAC, the sinc envelope attenuates the output signal:

$$V_{OU} = \frac{\sin\left(\pi f/f_s\right)}{\pi f/f_s}V_{REF}. \quad (8)$$

Noise power for the uncompensated DAC is same as for the compensated DAC. Thus, the maximum uncompensated-DAC SNR is

$$SNR_U = \frac{\sin\left(\pi f/f_s\right)}{\left(\pi f/f_s\right)}\frac{V_{REF}}{N_C}. \quad (9)$$

You can determine the degradation of the compensated-DAC SNR by dividing the SNRs:

$$SNR_C = \frac{\sin\left(\pi f_{MAX}/f_s\right)}{\left(\pi f_{MAX}/f_s\right)}\frac{\pi f/f_s}{\sin\left(\pi f/f_s\right)}SNR_U. \quad (10)$$

Degradation of the compensated-DAC SNR, unlike that of the uncompensated DAC, is frequency-dependent. Degradation is worse at frequencies lower than f_{MAX}.

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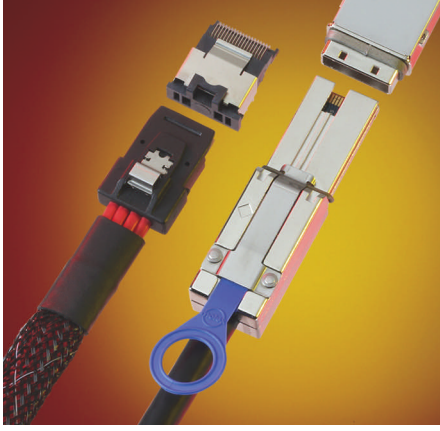

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POSTEQUALIZE?

Another method of equalizing the DAC's sinc-frequency response over the output-frequency band of interest is to add an analog filter whose frequency response is approximately equal to the inverse-sinc function. Many such analog-equalization filters exist for equalizing transmission lines and amplifiers, and you can adapt those equalization techniques for reducing the effect of a DAC's unwanted sinc response. The postequalization filter inserts after the DAC's reconstruction filter.

This application uses a simple active equalizer (**Figure 7**). For a given bandwidth, you choose R_1, R_2, and C_1 so that the analog equalizer's frequency response cancels the DAC's sinc-frequency response. Spice-simulation software can help optimize the frequency flatness for a given application. The frequency response for a typical analog equalizer shows that 0.1-dB flatness extends to more than 50% of $f_{NYQUIST}$. Without the postequalization filter, 0.1-dB flatness extends only to 17% of $f_{NYQUIST}$. Note that the maximum circuit gain is $1+R_1/R_2$.

A postequalization filter affects the DAC's SNR because it amplifies the noise at higher frequencies. Assuming that quantization noise limits the noise in an uncompensated DAC, the sinx/x envelope attenuates both the output signal and the noise. With a postequalization filter, however, the output-signal amplitude and noise density are constant over frequency, assuming perfect compensation. You obtain the output noise for the compensated and uncompensated DACs by integrating the noise power from near dc to $f_{NYQUIST}$:

$$N_C = \int_0^{f_{NYQUIST}} n_Q(f)|H(f)|\,df, \quad (11)$$

$$N_C = \int_0^{f_{NYQUIST}} n_{QO} \frac{\sin\left(\pi f/f_s\right)}{\pi f/f_s} \frac{\pi f/f_s}{\sin\left(\pi f/f_s\right)}\,df, \quad (12)$$

$$N_C = n_{QO} f_{NYQUIST}, \quad (13)$$

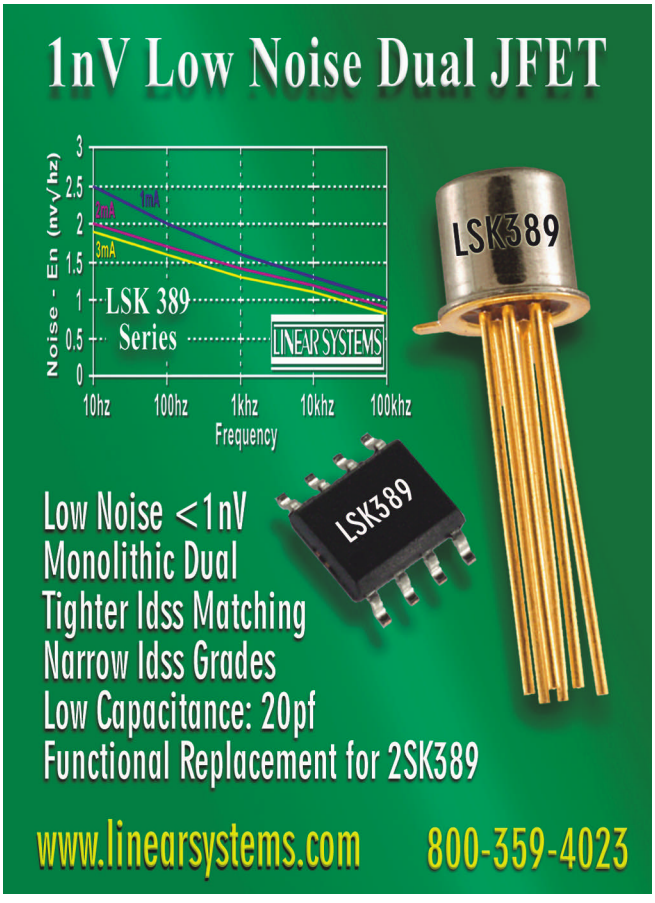
$$N_U = \int_0^{f_{NYQUIST}} n_Q(f)\,df, \quad (14)$$

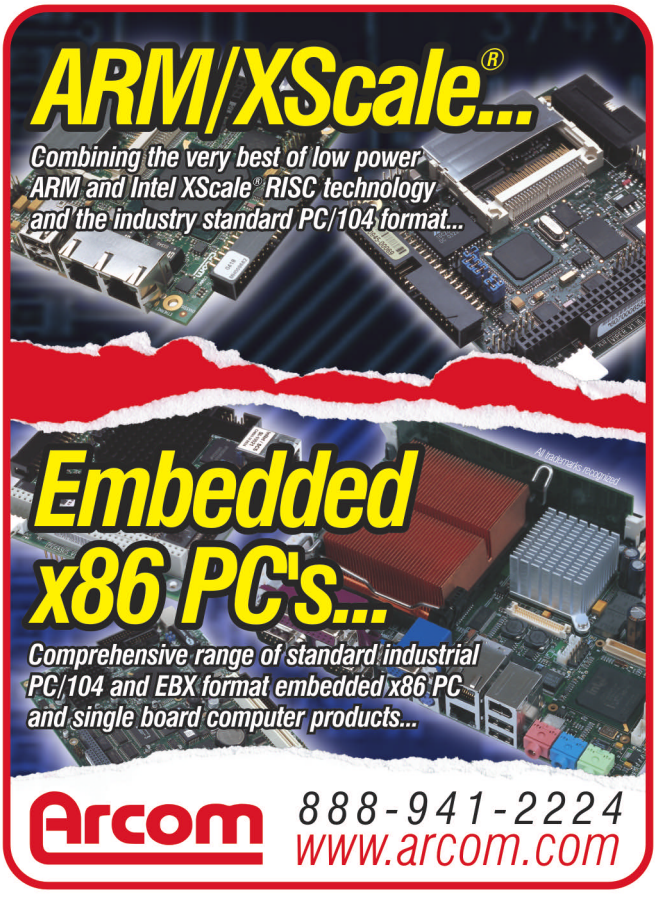
$$N_U = \int_0^{f_{NYQUIST}} n_{QO} \frac{\sin\left(\pi f/f_s\right)}{\pi f/f_s}\,df, \quad (15)$$

and

$$N_U = \frac{1.3708}{\pi} 2 f_{NYQUIST} n_{QO}, \quad (16)$$

where H(f) is the frequency response for the postequalization filter, $n_Q(f)$ is the noise power density, n_{QO} is the unattenuated quantization-noise density near dc, and N_C and N_U are the total noise power of the compensated and uncompensated DACs, respectively. Maximum SNR normalizes to the reference voltage, V_{REF}. Remember that $f_{NYQUIST}$ equals $f_S/2$. The SNRs are then:





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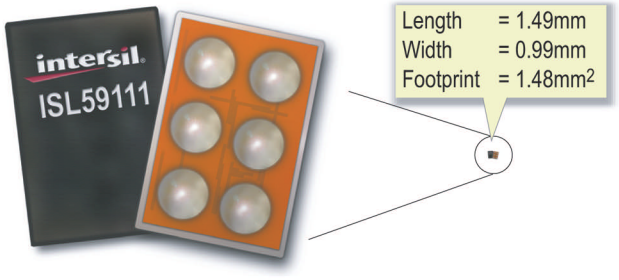

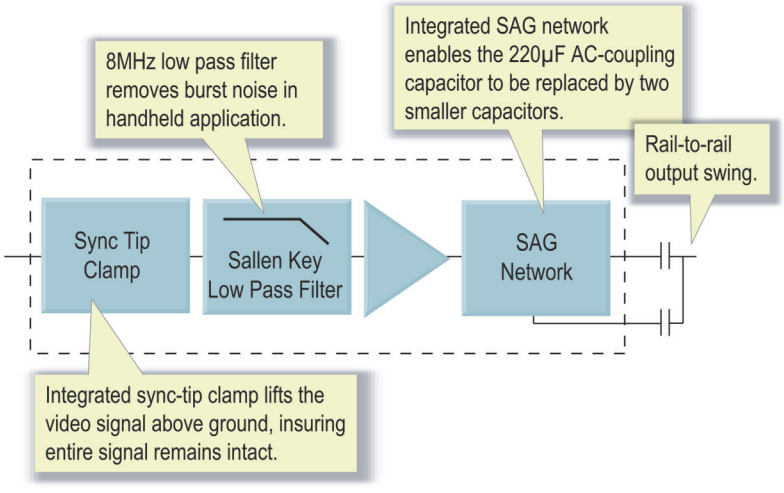

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$$SNR_C = \frac{V_{OC}}{N_C} = \frac{V_{REF}}{n_{QO} f_{NYQUIST}} \quad (17)$$

$$SNR_U = \frac{\frac{\sin\left(\pi f / f_s\right)}{\pi f / f_s} V_{REF}}{\frac{1.3708}{\pi} 2 f_{NYQUIST} n_{QO}}. \quad (18)$$

Again, dividing the two SNRs gives the compensated SNR in terms of the uncompensated SNR. The maximum SNR degrades at lower frequencies but improves at higher frequencies:

$$SNR_C = 2\frac{1.3708}{\pi}\frac{\pi f / f_s}{\sin\left(\pi f / f_s\right)} SNR_U. \quad (19)$$

So far, you assume that the DAC's reconstruction filter is an ideal lowpass filter: Its frequency response is flat to $f_{NYQUIST}$, and then it drops abruptly to zero. In practice, a reconstruction filter also adds roll-off near its cutoff frequency. Accordingly, the pre-equalization and postequalization techniques can serve an additional purpose of equalizing any roll-off in the reconstruction filter.

WRAPPING UP

The effect of a DAC's inherent sinc-frequency response attenuates output signals, especially at higher frequencies, and the resulting nonflat frequency response reduces the maximum useful bandwidth in broadband applications. Higher update rates flatten the frequency response but increase the DAC's cost and complexity.

The pre-equalization technique, which employs a digital filter to process the data before sending it to the DAC, offers 0.1-dB frequency flatness to 96% of $f_{NYQUIST}$ ($f_{NYQUIST}=f_S/2$) but requires additional digital processing. For comparison, an uncompensated DAC offers 0.1-dB flatness only to 17% of $f_{NYQUIST}$. Another technique adds a postequalization analog filter to equalize the DAC's output and achieves 0.1-dB flatness to 50% of $f_{NYQUIST}$ but requires additional hardware. Both compensation techniques offer a lower SNR at low output frequencies. EDN

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AUTHOR'S BIOGRAPHY

Until recently, Ken Yang was a senior member of the technical staff (applications) at Maxim Integrated Products. He obtained a bachelor's degree in physics from Washington State University (Pullman) and a master's degree in electrical engineering from the University of California—San Diego. He worked on a variety of products at Maxim, from simple voltage regulators to complex ADCs and multigigahertz microwave and RF devices.

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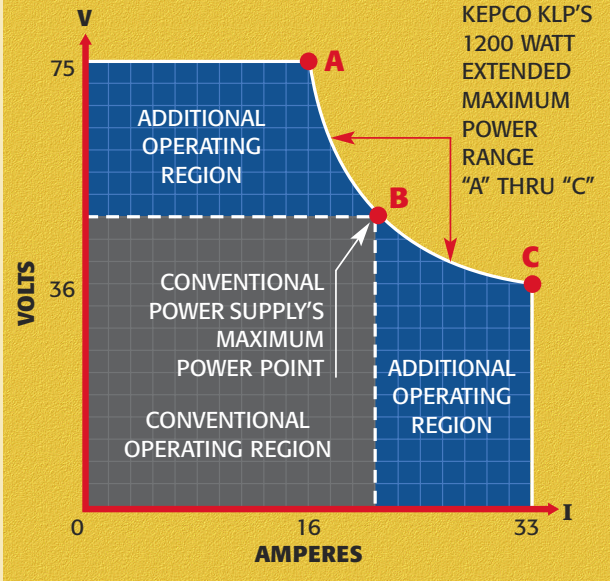

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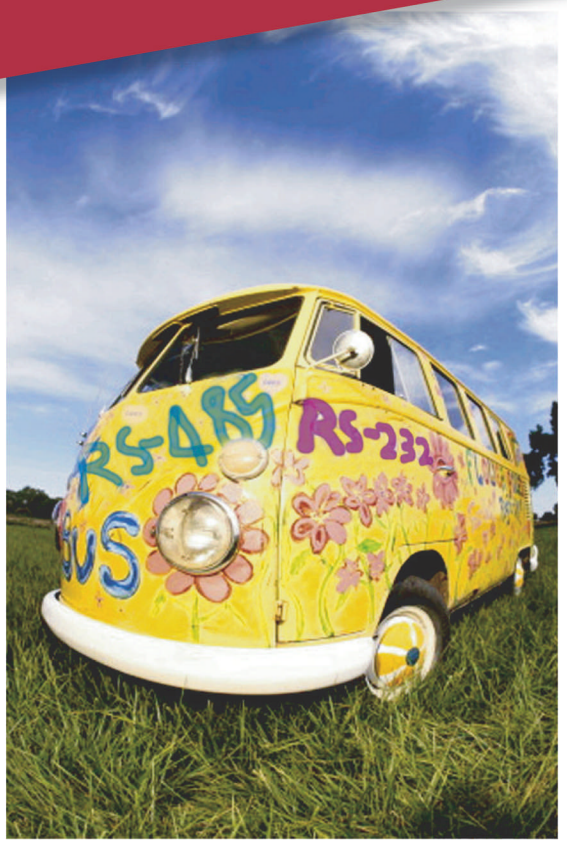

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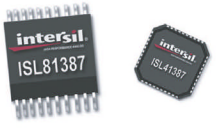

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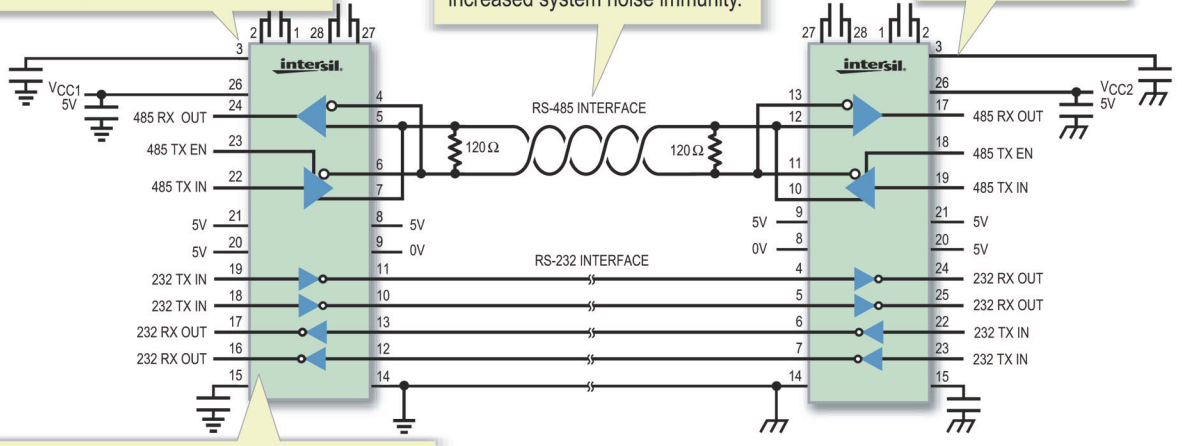

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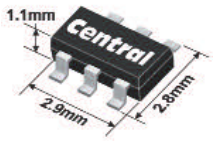

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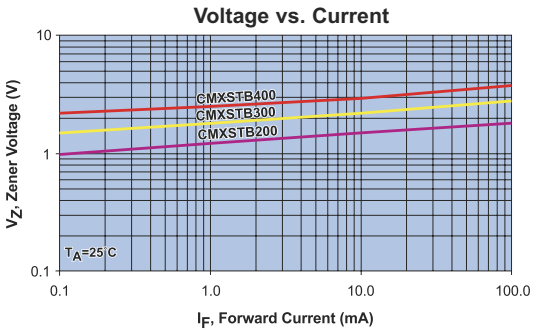

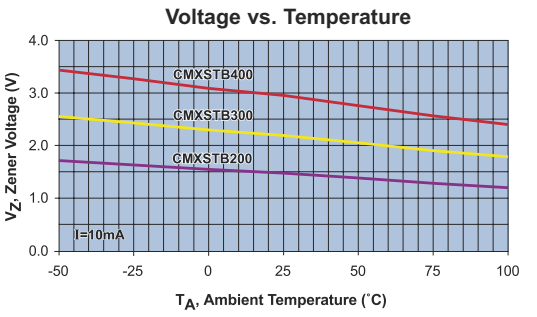

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LXI: Modular instrumentation for today and tomorrow

Agilent Technologies offers a test and measurement system that combines the best features of LAN technology and rack-and-stack instrument packaging

Modular instruments have become increasingly popular for building custom test systems. In a wide variety of settings—R&D, manufacturing, quality assurance, service and repair—these systems implement key setups for verifying, debugging and characterizing the designs of new products.

A few years ago, Agilent and VXI Technology (www.vxitech.com) became concerned about the limitations of the two leading modular-instrument packaging technologies—the venerable VXI (VME extensions for instrumentation) and the newer, and usually smaller, PXI (PCI extensions for instrumentation). PXI is based on CompactPCI, an embedded-systems packaging standard that is a ruggedized version of PCI (peripheral-component interconnect), which is widely found in desktop PCs.

Despite their popularity, those modular-instrument standards are hampered by several shortcomings that seem destined to become more onerous as time passes. First, both feature parallel buses that are becoming obsolete and that limit how far you can locate the modules from one another. Second, both are based on expensive shared power supplies and card cages responsible for cooling the modules that reside within the cages. Both also require that each card cage incorporate a costly Slot-0 module or system controller. Most important, although VXI and PXI rely on computer-industry buses, they have evolved into specialized standards that derive little benefit from the computer industry's high unit volumes.

Best of both worlds

What emerged from the discussions about modular instruments is LXI (LAN extensions for instrumentation). LXI combines the best of modular and rack-and-stack instrument packaging and brings other benefits of LAN technology to test and measurement. For example, LXI features Ethernet as the method for interconnecting rack-and-stack instruments in systems, instead of the venerable IEEE 488, a cabled parallel bus, also known as GPIB (general-purpose instrumentation bus).

IEEE 488 has served the T&M industry well over three decades, but its speed is no longer adequate for many applications. It is also routed through durable but large and expensive connectors and thick, balky cables. In contrast, Ethernet, operating at speeds to 10 Gbps, transmits its bus signals serially over thin, flexible, relatively low-cost cables terminated in inexpensive plastic-bodied RJ-45 connectors that snap together.To achieve physical consistency, the LXI standard begins with standard IEC (International Electrotechnical

Agilent Synthetic Instruments - LXI Class A (shown here).

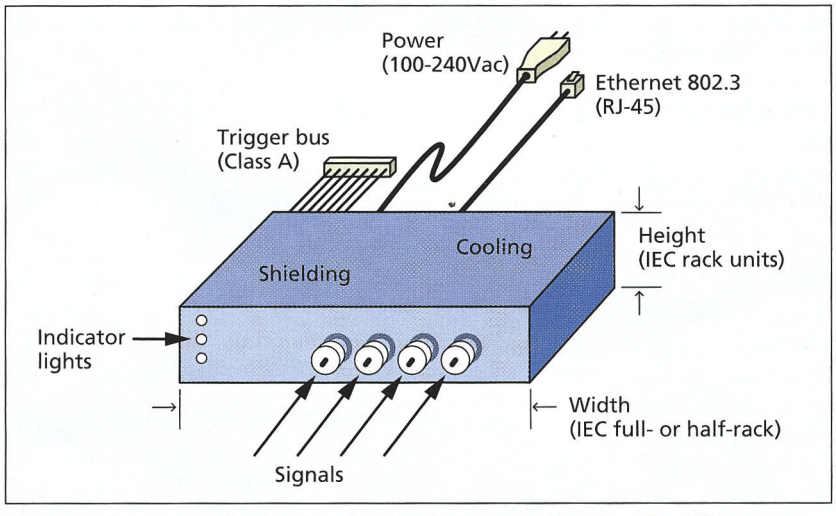

Figure 1. The LXI standard strives for physical consistency that simplifies system integration and implementation.

Commission) rack dimensions, but also defines an additional smaller instrument size of 1 LXI unit (1U high—that is, 1.75-in.-and ½-rack wide). The standard also recommends the placement of various connections (Figure 1). For example, compliant instruments use the front panel for signal inputs and outputs, plus indicator lights for LAN, power, and IEEE 1588 (synchronization). The rear panel contains connectors for hardware triggering, power input, and Ethernet communication. Each LXI module must meet worldwide standards for cooling and EMI (electromagnetic-interference) shielding. LXI modules receive operating power either from the ac line or, by use of POE (power over Ethernet) technology, from the network connection.

By specifying the interaction of proven, widely-used standards such as Ethernet, Web browsers, and IVI (interchangeable virtual instrument) drivers, LXI enables fast, efficient and cost-effective creation and reconfiguration of test systems. Other benefits include: compact size and higher test throughput than are found with rack-and-stack instruments or caged instrument modules. Agilent and the more than 40 corporate members of the LXI Consortium believe that these LXI-based test systems are "future proof." They won't become obsolete any time soon.

More than just a LAN port

Although many current-generation instruments include LAN ports, LXI is the next logical step in the evolution of LAN-based instrumentation. It includes classic "box" instruments, modular instruments without panel-mounted controls and displays, and functional building-block modules (synthetic instruments). Even when space is at a premium, you don't have to sacrifice capability, accuracy, or performance. Best of all, you can use the same instruments—and leverage the same test-system software—across R&D, design validation, manufacturing, and service. Using the same hardware and software in these disparate activities not only cuts test-development time, but it also results in more consistent measurements and less time wasted in trying to correlate measurements made by different people in different places.

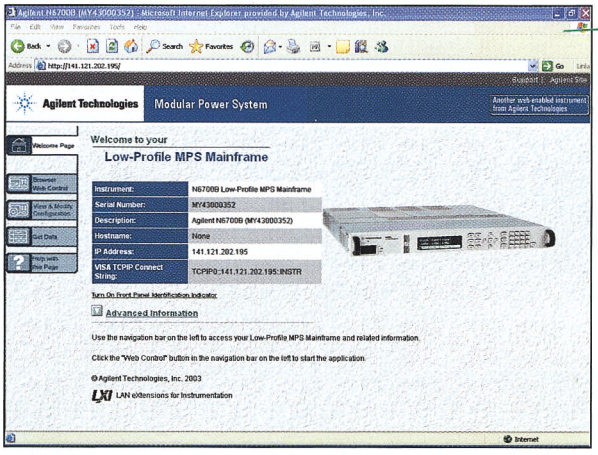

Figure 2. LXI specifies an informative instrument page that engineers can access with a standard Web browser.

Every LXI-compliant device must also be able to serve its own Web page. This page provides key information about the device, including its manufacturer, model number, serial number, description, hostname, MAC (media-access control) address and IP (Internet Protocol) address (**Figure 2**). The standard also requires a browser-accessible configuration page that allows the user to change parameters such as hostname, description, IP address, subnet mask, and TCP (transfer-control protocol)/IP-configuration mode. Accessing these Web pages is as simple as typing the instrument's IP address into the address line of any standard Web browser.

Many of Agilent's LXI-compliant instruments go beyond the LXI requirements, providing monitor and control capabilities in their Web pages. For example, you can set up a DMM (digital multimeter), command it to start making measurements and then read the results. The ability to control an instrument through a browser interface opens a realm of new possibilities for test engineers who need a simple way to access test systems from virtually anywhere in the world.

Triggering options

One especially intriguing aspect of LXI is its triggering and synchronization capabilities. By harnessing the capabilities of the LAN and the IEEE 1588 time-synchronization protocol, LXI provides a variety of triggering modes that are not available in GPIB, PXI, or VXI.

The three classes of LXI devices—Classes C, B, and A—implement these capabilities to an increasing degree. Class C provides the basic capabilities associated with LXI instruments. Class B adds LAN triggers and time-based triggers using the IEEE 1588 precision time protocol (both over LAN). In addition, Class A features a hardware trigger bus that enables triggering of LXI instruments in close proximity. The trigger bus is similar to the backplane bus of VXI. It is an eight-pair, differential-voltage bus that enables 5-nsec/m timing accuracy for co-located instruments. Synthetic instruments are expected to comply with Class A.

Combine this triggering flexibility with such benefits as high performance, compact size, and web-based control, and it is easy to see why LXI is increasingly becoming the engineer's best option for effective modular instruments. ■

FOR MORE INFORMATION

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BY WOLFGANG MAICHEN, PHD • TERADYNE INC

Easing the modeling of lossy lines

SIMPLE MEASUREMENTS AND STRAIGHTFORWARD TECHNIQUES NOT ONLY CAN OFTEN OBVIATE THE NEED FOR EXPENSIVE SIMULATION TOOLS, BUT ALSO CAN PROVIDE A MORE INTUITIVE FEEL FOR NETWORK BEHAVIOR.

With common data rates quickly entering the gigabit-per-second domain, frequency-dependent losses in interconnects—cables and pc-board traces—are quickly becoming major obstacles to further speed increases. Thus, you can no longer ignore transmission losses; during system development as well as for device and system test, timing-budget planning requires accurate modeling of these losses.

Today, you can buy a variety of software—both for RF- and time-domain (usually digital) applications—to predict those losses and to build equivalent-circuit models based either on theoretical calculations or on actual measurements. Although powerful for experienced engineers, these tools have two severe downsides for engineers who need only occasionally to build usable models with a minimum of effort: First, the tools are expensive, making it difficult to justify their cost. Second, the more powerful their features, the more arduous their learning curve, so designers cannot be productive with them without spending a lot of time using them—again an important obstacle for an engineer whose main task is something other than transmission-path modeling.

This article describes an easy-to-follow measurement-based method for creating practical models for lossy cables and pc traces, using nothing but easily available and inexpensive Spice and Excel software tools. As an added advantage, you will gain insight into the effect and behavior of those losses. In the end, it is more rewarding to solve a problem in a pedestrian way than to plug data into a program and then mindlessly believe the results it produces.

LOSSY TRANSMISSION LINES

Figure 1 shows the general model of a lossy transmission line: Its components are the series inductance L, shunt capacitance C, series resistance R, and shunt conductance G. For a homogeneous transmission line, those parameters are distributed evenly along the length of the line. For an ideal lossless transmission line, R and G are zero. (Note that R is a resistance, which you measure in ohms, and G is a conductance, which you measure in siemens=1/ohms.) A frequency-dependent R_F models ohmic resistance and skin-effect loss. The skin-effect loss is nothing other than ohmic resistance aggravated by the inhomogeneous current distribution that results from the skin effect. Frequency-dependent G_F represents dielectric losses. This frequency dependency causes all of the trouble in modeling signal propagation. The general expression for the characteristic impedance, Z_0, of this line is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}, \quad (1)$$

and $\omega = 2\pi f$ (**references 1** and **2**). For sufficiently high frequencies, relatively small losses, or both ($R << \omega L$, and $G << \omega C$), you can approximate this expression as:

$$Z_0 = \sqrt{\frac{L}{C}}. \quad (2)$$

This **equation** is the same as that for a lossless transmission line. Practical digital interfaces all fall into this range. This piece of information is important because it tells you that—apart from some signal attenuation—the signal propagation is the same as for lossless lines. For example, Z_0 is largely independent of frequency, and the following expressions hold:

$$\begin{aligned} T_{PD} &= \sqrt{LC}; \\ L &= T_{PD} \times Z_0; \quad \text{and} \\ C &= T_{PD} / Z_0. \end{aligned} \quad (3)$$

Here, T_{PD} is the propagation time through the line (**Reference 1**). This set of **equations** allows you to determine model parameters—in this case, L and C—based on measurements of propagation time and characteristic impedance. The general propagation constant of a lossy line is:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L) \times (G + j\omega C)}, \quad (4)$$

where α (the real-valued part) describes the signal attenuation, and $j\beta$ (the imaginary part) describes the wave propagation along the line. Under the same low-loss assumptions as before, **Equation 4** approximates to:

$$\begin{aligned} \alpha &\approx \frac{1}{2} \times \left(\frac{R}{Z_0} + G Z_0 \right); \\ \beta &\approx \omega \times \sqrt{LC} = \omega \times T_{PD}. \end{aligned} \quad (5)$$

For a lossless line, α is zero. An important conclusion from α in **Equation 5** is that the signal gain through a lossy line is:

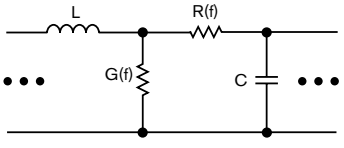


Figure 1 In the general model of a lossy transmission line, its components are the series inductance L, shunt capacitance C, series resistance R, and shunt conductance G.

$$GAIN = \frac{V_{OUT}}{V_{IN}} = e^{-\frac{R}{2Z_0}} \times e^{-\frac{GZ_0}{2}}, \quad (6)$$

where V_{IN} and V_{OUT} are the signal amplitude entering and exiting the line, respectively. Although transmission theory usually talks in terms of gain, in this case, the gain is always less than one, so it is really a loss. **Equation 6** is the third formula you need to build a model, because it relates the measured loss through a cable or trace to the loss parameters R and G. Because gain or loss can span a wide range of magnitudes, it is usually stated in the logarithmic decibel scale. Thus,

$$GAIN_{dB} = 20 \times \log(GAIN) = -20 \times \log(e) \times \left(\frac{R}{2Z_0} + \frac{GZ_0}{2}\right);$$
$$LOSS_{dB} = -GAIN_{dB}. \quad (7)$$

LOSS MODELS

The only piece of theory still missing is a set of models for the behavior of the different loss contributors versus frequency. The easiest is ohmic dc loss, because it does not depend on frequency. It forms one part of the series resistance R, and is denoted as R_{DC}. Skin effect causes the second part of the series resistance. For a perfect coaxial cable, the skin resistance is proportional to the square root of the frequency, and you can even derive an analytical expression for the proportionality factor (**references 1** and **2**). For arbitrarily shaped transmission lines, such as striplines in a pc board in which the field distribution is more complicated, this approach no longer works, but the square-root behavior remains at least approximately valid. Thus, you can model the series resistance due to skin effect as:

$$R_{SKIN} = k_{SKIN} \times \sqrt{f}. \quad (8)$$

For these purposes, the factor k_{SKIN} is simply a fit parameter, which you adjust to match the measured behavior. The skin resistance and the dc resistance add to the total resistance to produce:

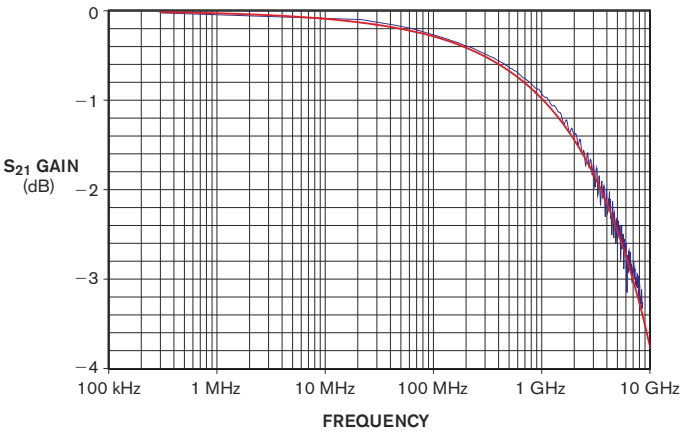


Figure 2 In this comparison of the measured-loss curve and the model-simulation results, the match is excellent over the whole range, especially considering that the model comprises just one circuit element in PSpice.

$$R = R_{DC} + R_{SKIN}. \quad (9)$$

This **equation** is only a rather crude approximation, but, as you will see later, it greatly simplifies fitting the loss behavior to the measured data. **Reference 2** mentions that you can achieve a better fit to the actual resistance trend by taking the root-mean-square of R_{DC} and R_{SKIN}—that is, $R = \sqrt{(R_{DC}^2 + R_{SKIN}^2)}$.

Finally, dielectric losses—represented by the shunt conductance, G—increase approximately linearly with frequency. This rule is just an approximation, because, for any real-world dielectric material, the loss tangent, tanδ, varies somewhat with frequency, although the variation is much smaller than the frequency variation. That is,

$$G = 2\pi \times f \times C \times \tan\delta = k_{DIEL} \times f = k_{DIEL} \times \left(\sqrt{f}\right)^2. \quad (10)$$

You'll soon see the advantage of the strange square-root formulation. Just as for the skin effect—because you usually don't know the effective loss tangent—k_{DIEL} is a fit parameter that you adjust to best fit the measurement.

You can now insert those loss models into the general expression for the total line losses:

$$GAIN_{dB}(f) = -20 \times \log(e) \times \left(\frac{R_{DC}}{2Z_0} + \frac{k_{SKIN}}{2Z_0} \times \sqrt{f} + \frac{Z_0 k_{DIEL}}{2} \times \left(\sqrt{f}\right)^2\right). \quad (11)$$

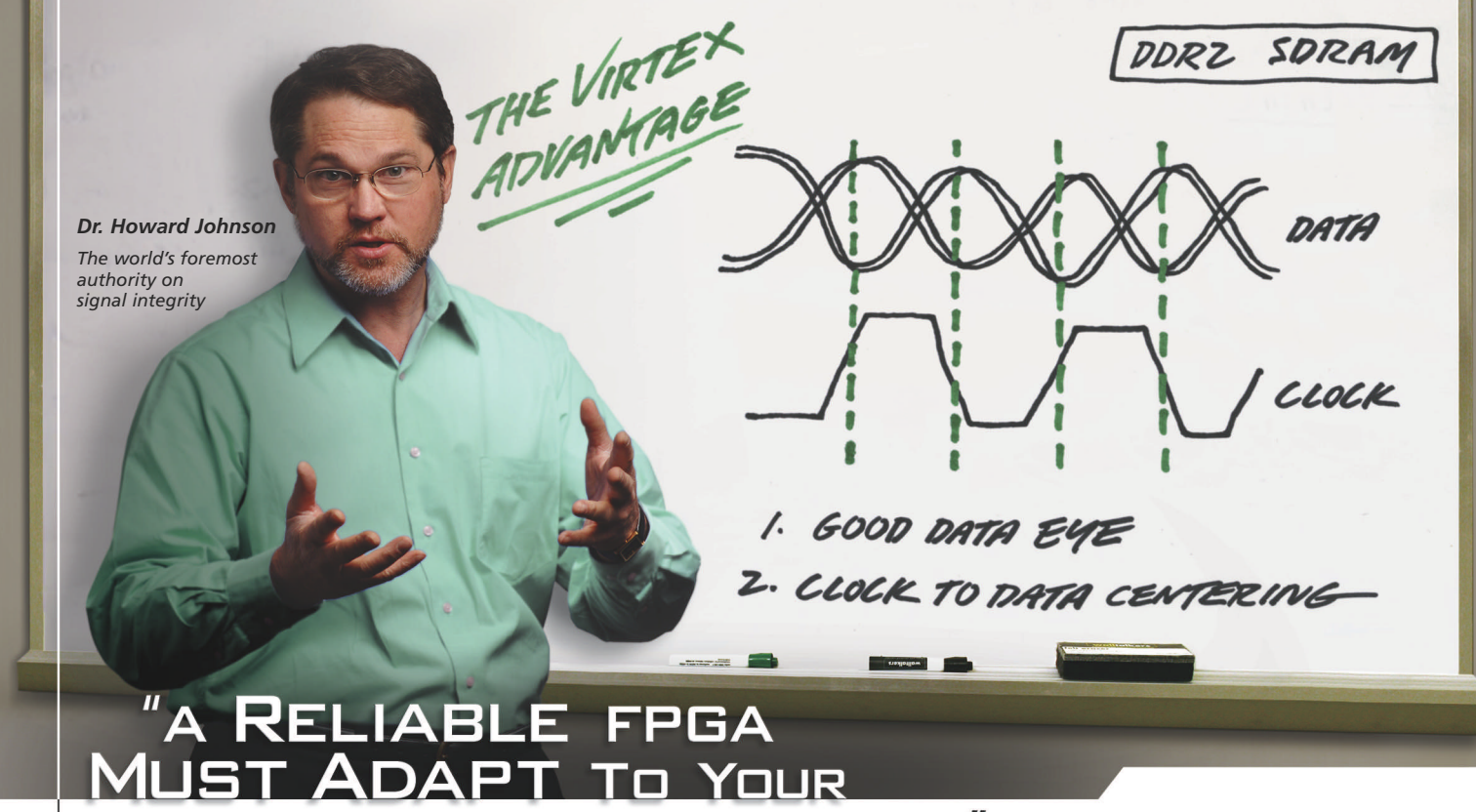
If you look closely, you see that—if you plot the measured gain in decibels versus the square root of the frequency instead of the frequency itself—the equation reduces to a simple parabola:

$$GAIN_{dB}(x) = a + bx + dx^2.$$
$$x = \sqrt{f}.$$
$$a = -20 \times \log(e) \times \frac{1}{2Z_0} \times R_{DC}. \quad (12)$$
$$b = -20 \times \log(e) \times \frac{1}{2Z_0} \times k_{SKIN}.$$
$$d = -20 \times \log(e) \times \frac{Z_0}{2} \times k_{DIEL}.$$

In other words, once you have measured the loss in decibels over a range of frequencies, the actual data fitting becomes almost trivial. One possibility is to use Excel for this task, because almost every engineer has it readily available, and it can perform polynomial fits. But any other fitting software will also do the job. From the fit parameters a, b, and d, you can then easily calculate the loss parameters R_{DC}, k_{SKIN}, and k_{DIEL}.

MEASUREMENT AND MODEL-BUILDING

For practical measurements, a VNA (vector-network analyzer) is the tool of choice. A scalar network analyzer will do just fine for the loss measurement, but you will need to determine the propagation delay, T_{PD}, with some alternative method, such as TDR (time-domain reflectometry). If no network analyzer is available, you can measure the attenuation using a sine-wave source (an RF generator) and an oscilloscope, though it is a bit tedious to acquire a sufficient number of points, and accurate measurement of small losses is difficult. The reasons that it is better to do the modeling in the frequency domain are



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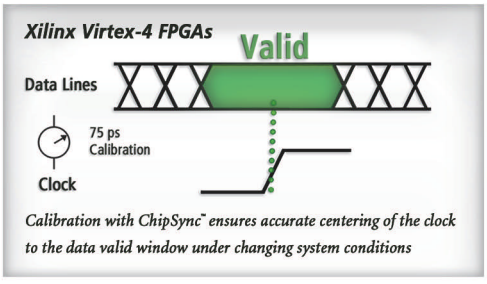

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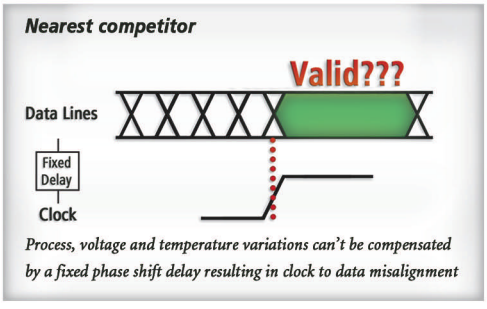

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twofold: First, losses have an easy-to-describe behavior in the frequency domain, in contrast with rather difficult-to-interpret time-domain behavior (for example, step response). Second, VNAs have unparalleled amplitude-measurement—and, therefore, loss—resolution, which can cover the whole range, from very small to very large losses. (A VNA can easily reach an SNR of 100 dB—a factor of 10^5, whereas an oscilloscope is hard-pressed to reach even 60 dB—a factor of 10^3.) Nevertheless, the resulting Spice model is not restricted to frequency-domain simulations (ac sweeps). Rather, it performs just as well in a time-domain simulation (transient response).

You need to set the frequency sweep to logarithmic and measure the absolute value of the transmission coefficient, S_{21}—plotted on a decibel scale. S_{21} is then identical to the gain in decibels from before. (Note that S_{21} is a complex value; it has both magnitude and phase.) You then transfer the data to a computer equipped with Excel or some other plotting program, replot the curve versus the square root of the frequency, and use **Equation 12** to fit the curve to the data and to obtain R_{DC}, k_{SKIN}, and k_{DIEL}. The choice of frequency sweep—linear or logarithmic—has a slight influence on the fit result: A linear sweep overemphasizes the high-frequency range, whereas a logarithmic sweep distributes the measured data points evenly over the whole range.

Next, change the VNA setup to display the group delay of S_{21}. The group delay is defined as the derivative of the phase, ϕ, over the frequency, f. That is,

$$T_G = \frac{d\varphi}{df}. \quad (13)$$

For dispersionless paths, the group delay has a simple meaning; in those cases, it is identical to the propagation delay, T_{PD}, of the path. Fortunately, this scenario normally closely approximates the real situation. The condition for constant group delay is that the dielectric constant, ϵ, does not vary with frequency. The dielectric constant can be truly frequency-independent only

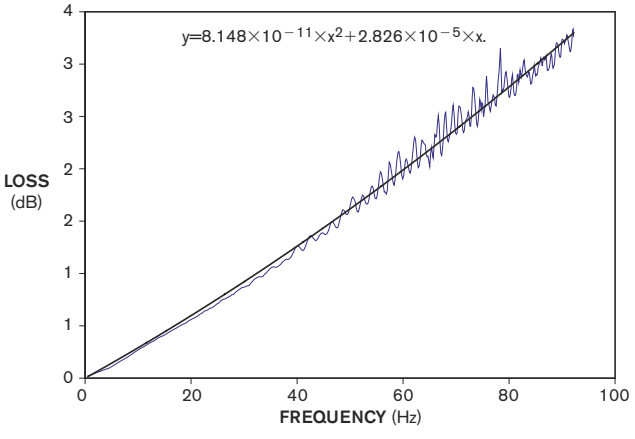

Figure 3 In the parabolic fit and the resulting fit parameters, the dc resistance is negligible; so, in the fit, the y intercept is set to zero.

TO MINIMIZE THE IMPACT OF FRINGE EFFECTS, ALWAYS START WITH THE LONGEST CABLE OR TRACE AVAILABLE.

for lossless media; whenever losses occur, the dielectric constant changes over frequency (governed by the so-called Kramers-Kronig relation). (If the VNA does not offer the option to display the group delay directly, you can instead display the phase. You then calculate the group delay from the slope of the phase curve.) One potential trap is that the VNA calculates the group delay numerically, based on the phase difference between adjacent data points. If the frequency spacing between points is too large, this approach can yield erroneous results because the phase wraps around every 360°. To avoid this problem, you need to ensure that the VNA sweep uses sufficiently closely spaced points. A simple test is to double the number of points and verify that the displayed group-delay curve does not change. The group-delay display usually yields useful readings only in the region above 100 MHz; for lower frequencies, the phase change is small because the wavelength is much longer than the propagation time, and measurement noise and other inaccuracies thus heavily impact the result. You usually know the path impedance, Z_0, from pc-board design parameters or the cable data sheet. In digital applications, it is almost without exception 50Ω. Thus, you can calculate the total line capacitance, C, and the total line inductance, L, using **Equation 3**.

A few more measurement hints may be useful. First, to minimize the impact of fringe effects, always start with the longest cable or trace available. In other words, path loss must dominate effects of impedance mismatches at the connection points at both ends of the cable or trace—for example, SMA connectors or probes. Otherwise, characterization and mathematical de-embedding of those connectors, which go far beyond the scope of this article, become necessary. This area is one in which professional modeling tools are useful. Second, use the widest frequency range available—as low and as high as the VNA can go—because the wider the range, the more reliable the curve fit will be. It is always more accurate and reliable to interpolate than to extrapolate, although one of the benefits of this fitting method is that it allows you to confidently extrapolate losses beyond the measured range if necessary. Ideally, you should go to at least twice the highest frequency present in the signal—that is, to at least twice the signal bandwidth. For a digital signal, the signal's 10 to 90% rise time, rather than the data rate or clock frequency, gives the approximate bandwidth:

$$BW \approx \frac{0.33}{T_{R,10/90}}. \quad (14)$$

Spice is a popular simulation tool. Among Spice variants, Orcad's PSpice is a good choice because it offers a lossy-transmission-line model as a built-in library component, and a free, fully functional, downloadable demo version is available that restricts only the number of components you can use (**Reference 3**). The fact that the download is free greatly reduces the cost of getting started if you want to try modeling. The only issue

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is that PSpice does not offer frequency as a parameter for lossy lines but instead provides the Laplace parameter, $s=2\pi jf$. You can quickly overcome this limitation by substituting:

$$f = \mathrm{abs}\left(\frac{s}{2\pi}\right), \quad (15)$$

In addition to the parameters C, L, R, and G, the lossy-transmission-line model in PSpice offers the LEN (length) parameter. Because the calculated parameters refer to the total line, you can simply set LEN to 1. After you model the line, this parameter provides a way to scale the model up or down for different line lengths—for example, you have measured a long line to minimize connector effects but want to build a model for a shorter section of the same type of line. Finally, if you want to use formulas for parameters in PSpice, you must enclose them in braces.

If you have no access to the far end of the line because, for example, it ends in a socket or in a needle-probe head, you can't make transmission measurements. The easy solution is to measure the reflected signal, S_{11}, instead of S_{21}, because doing so requires only one connection to one end of the line. For this approach to work, the line's other end—that is, the far end—must remain unterminated. The signal then traverses the line, is fully reflected at the far end, and returns to the source, so it effectively traverses the line twice. Data collection and fitting occur as usual. The only difference is that you must halve all measured values to represent a single traversal. This procedure neglects the effect of the parasitic fringe capacitance that can differ when the line is open compared with when it is terminated at the far end.

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AN EXAMPLE

The following example applies the theory to a practical situation. The object to be modeled is a coaxial cable with an SMA connector on each end. The intended signal bandwidth is approximately 2 GHz. The VNA's frequency range—300 kHz and 8.5 GHz—is sufficient for this application. You need to take care in calibration, however, because even slight errors affect the accuracy of the measured parameters, especially in the low-frequency region in which the losses are small.

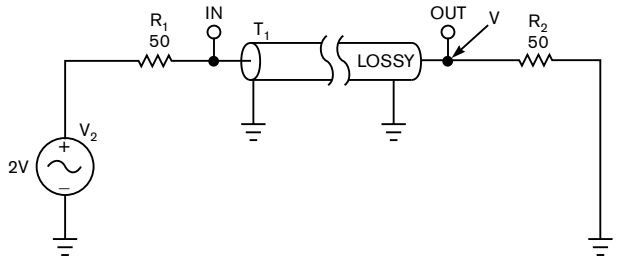

Figure 4 In the PSpice model for simulation, to match the VNA measurements, you must terminate the lossy line with a matched 50Ω termination, and the ac sine-wave source also must have 50Ω output impedance.

Figure 2 shows the measured loss curve as well as the model-simulation results. The match is excellent over the whole range, especially considering that the model comprises just a single circuit element in PSpice. The slight wiggle at high frequencies is due to reflections at the connector discontinuities, which the model does not include and therefore can't reproduce in the simulation. **Figure 3** shows the parabolic fit and the resulting fit parameters. The dc resistance is negligible, and thus the curve fit omits it by setting the y intercept to zero. For the measured and fitted parameters, Z_0 is 50Ω, which you know and have verified with TDR; T_{PD} is 2.8 nsec, which you know and have verified using group delay or TDR; a is zero, with negligible dc losses; b is 2.826×10^{-5} from the curve fit; and d is 8.148×10^{-11}, also from the curve fit.

From this formula, you can calculate the model parameters for the lossy cable using **equations 3**, **12**, and **15**: LEN=1, C=56 pF, L=140 nH, R={$3.254\times10^{-4}\times\sqrt{\mathrm{abs}(s/2\pi)}$}, and L={$3.752\times10^{-13}\times\mathrm{abs}(s/2\pi)$}.

Figure 4 also displays these parameters along with the PSpice model used for simulation. To match the VNA measurements, you must terminate the lossy line with a matched 50Ω termination, and the ac sine-wave source also must have 50Ω impedance. Even though the plot is a frequency-domain sweep, you could just as easily use the same PSpice model for time-domain transient simulations without any changes to the model itself.

If you are interested in the quality of the cable's dielectric, you can determine the loss tangent using **Equation 10** with C=56 pF and $k_{DIEL}=3.752\cdot10^{-13}$:

$$\tan\delta = \frac{k_{DIEL}}{2\pi\times C} = 0.0011, \quad (16)$$

which shows that the dielectric is indeed a very-low-loss material.

If your Spice version offers no built-in lossy-transmission-line models, you can use these parameters for the whole line and divide them into a chain of small, lumped sections from discrete elements (**Figure 1**). However, the simulator must be able to accept frequency-dependent values for R and G, and this requirement will likely be a breaking point for many simulation tools. To avoid model artifacts, the propagation time through each lumped section should be smaller than about one-tenth of the fastest signal rise time for which the model shall be valid. In other words, the number of those sections should be at least

$$N \geq 10\times\frac{T_{PD}}{T_R}, \quad (17)$$

and the component values for each section are:

$$C_I = \frac{C}{N}, L_I = \frac{L}{N}, R_I = \frac{R}{N}, G_I = \frac{G}{N}. \quad (18)$$

SUMMING UP

You can create highly usable, accurate models of lossy transmission lines, including cables and pc-board traces, using only a minimum of mathematics and readily available tools—a VNA,

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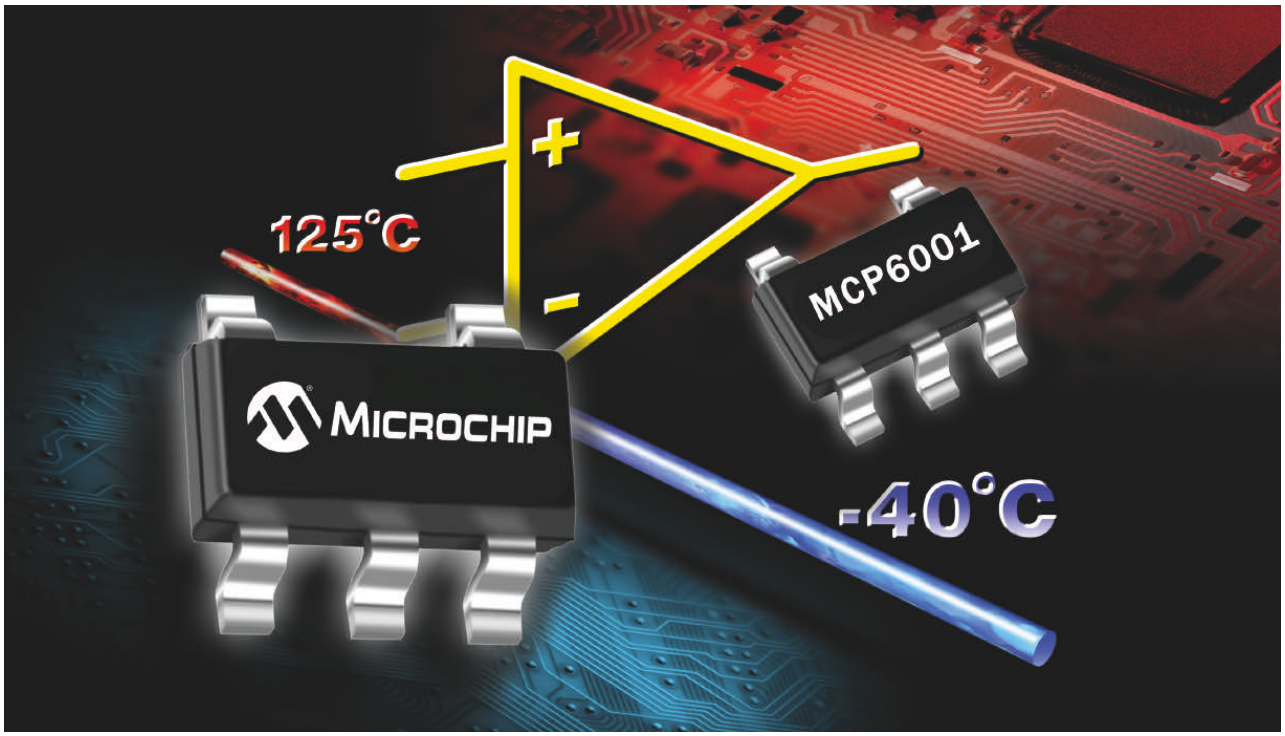

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MCP6141/2/3/4	100 kHz	0.6	3.0	170	1.4 – 5.5
MCP6231/2/4	300 kHz	20	5.0	52	1.8 – 5.5
MCP6241/2/4	550 kHz	50	5.0	45	1.8 – 5.5
MCP6001/2/4	1 MHz	140	4.5	28	1.8 – 5.5
MCP6271/2/3/4/5	2 MHz	170	3.0	20	2.0 – 5.5
MCP6281/2/3/4/5	5 MHz	445	3.0	16	2.2 – 5.5
MCP6291/2/3/4/5	10 MHz	1100	3.0	8.7*	2.4 – 5.5
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Excel, and PSpice—and following a simple recipe; you simultaneously gain understanding about loss behavior. An extension of the method would include approximate models of the connectors. A lumped capacitance or inductance often suffices, and you can analytically add it to the fitting process without recourse to numerical modeling, but you must experimentally determine the numerical values—either through TDR or time-domain transformation of the VNA data. Using the root-mean-square sum for skin resistance and dc resistance could also improve the quality of the fit parameters at the cost of making the fit nonpolynomial, which would require more elaborate fit routines. However, for most applications, the method is likely to provide more than adequate model accuracy and is easy to implement on a variety of fit and modeling tools.

Finally, many engineers working with digital signals have no access to a VNA but have oscilloscopes that can perform time-domain-transmission measurements; in such cases, you can harness step-transmission data to get the loss parameters through Fourier conversion of the time-domain data into S-parameters **(Reference 4)**.EDN

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Wolfgang Maichen is an IC-characterization engineer at Teradyne Inc (Agoura Hills, CA). His interests center on measurement techniques, signal integrity, benchtop characterization of high-speed digital and mixed-signal ASICs, time-domain reflectometry, and system-timing accuracy. Before joining Teradyne, he worked as a product engineer for Siemens Semiconductor (now Infineon) in France. Maichen holds a master's degree and a doctorate in applied physics from the University of Technology (Graz, Austria). He has published several papers in international peer-reviewed journals and regularly gives presentations and tutorials at international conferences. He is an invited author for the book Advances in Electronic Testing, *edited by Dimitris Gizopoulos. He is working on his own book,* Digital Timing Measurements, *which is due out in May.*

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ACROSS

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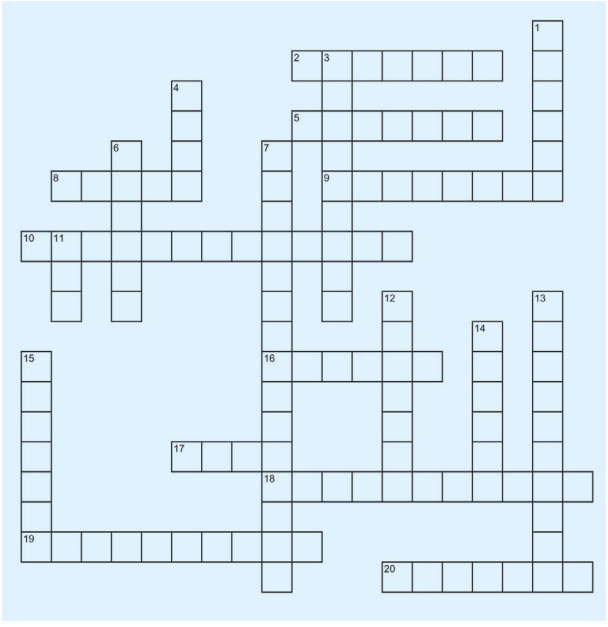
5 He helped to derive mathematical operations that transforms a signal from the time domain to the frequency domain, and vice versa
8 Unwanted signals
9 A measure of the capability of a DAQ system to faithfully indicate the value of the measured signal
10 Containing one or more type of I/O operation on a single device
16 Annual conference of virtual instrumentation held in Austin, TX
17 A semiconductor device containing programmable logic components that can be reprogrammed based on varying functionality requirements
18 Devices that convert a physical phenomenon into a measurable electrical signal
19 18 bits of this provides 262,144 discrete levels
20 He helped discover that a signal must be sampled at least twice as fast as the bandwidth of the signal to accurately reconstruct a signal



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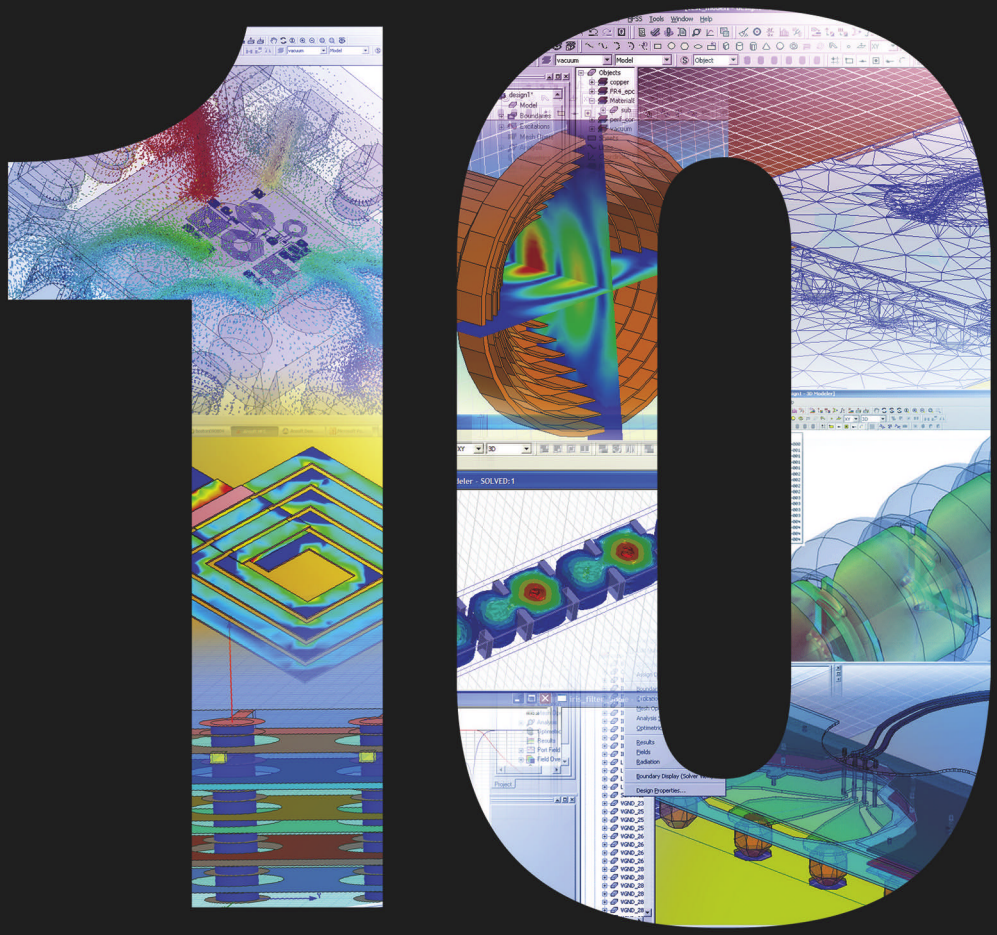

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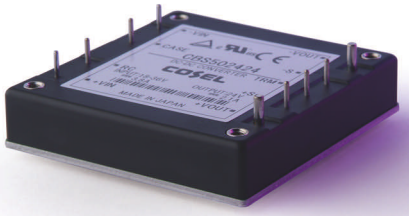

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Multiprocessor architectures tackle tough processing demands

OPTIMIZE POWER AND PERFORMANCE WITH A MULTIPROCESSOR SOC APPROACH.

High-performance applications, such as multifunction intrusion-detection and firewall-security functions in enterprises and high-speed protocol processing in wireless and storage networks, including PPP (Point-to-Point protocol), iSCSI, and TCP (Transmission Control Protocol) termination, increase processing demands in two dimensions. A system must not only handle more data, but also perform deeper packet processing. Today's engineers face the daunting challenge of implementing the significant increase in processing capabilities for these applications and keeping power dissipation under control.

Traditionally, engineers increase the processor-clock frequency to achieve higher performance levels. However, frequency scaling is no longer the panacea for increasing performance because devices hit the "power wall," at which transistors leak as much current when they are inactive as when they are active. For example, Intel's (www.intel.com) Pentium processor at 4 GHz operates at 100W.

At some point, frequency scaling reaches a point of diminishing or negative returns as internal chip architectures begin to break down (**Figure 1**). Processors become I/O- or memory-bound as architectural resources become more unbalanced, which limits the achievable performance gains. To scale performance without breaking power budgets or processor architectures, innovation must occur beyond scaling the manufacturing process.

A common approach to increasing performance has been to leverage SOC (system-on-chip) integration and hardware acceleration. When optimizing performance, designers must adhere to a strict power budget; sometimes, reducing the clock frequency further reduces power. For many applications, running multiple processors at a lower clock speed can provide performance equivalent to and consume significantly less power than that of a single high-frequency processor. For example, four 1-GHz cores can provide the same performance as a single 4-GHz core. With each 1-GHz core operating at 3W, a quad-core architecture consumes 12W, or 12% of the power a 4-GHz Pentium requires.

To achieve optimal performance, developers must combine these approaches to improve performance and power efficiency. In some cases, changes in design methodology, such as fine-grained clock gating, are appropriate. Moving to a multiprocessor architecture requires rethinking SOC design, especially with highly integrated SOC devices, because the bottlenecks for board-level systems vary greatly from those for chip-level systems. From a software perspective, executing an application across multiple cores requires application partitioning, efficient use of available hardware-acceleration resources, robust interprocessor-communication mechanisms, and contention avoidance for shared resources. Additionally, applying dynamic power management at the application level can achieve considerable power savings.

RETHINKING INTEGRATION

With advances in SOC manufacturing, designers can integrate an entire multiprocessor subsystem onto a single chip. The collocation of components within the same device produces immediate and direct benefits for reducing latency between components and better control of contention and coherency.

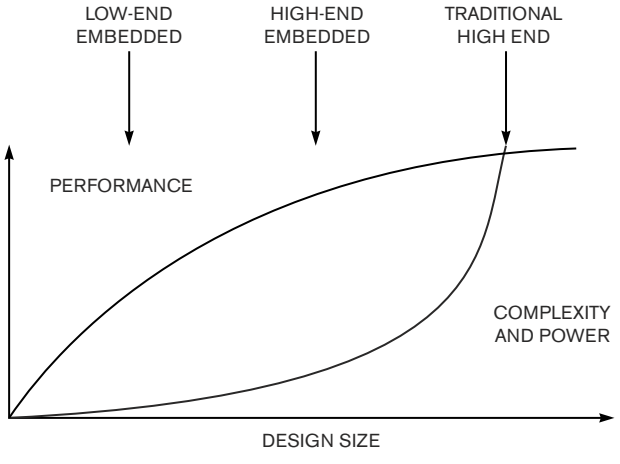

Figure 1 As performance increases in single-core architectures, so does design complexity and power consumption. With increasing frequency scaling, processor architectures eventually hit the power wall, at which transistors leak as much current when they are idle as when they are active.

Reducing latency increases overall performance, and managing coherency eases programming complexity and improves performance. The approach yields other immediate power savings because signals need to travel across only the chip rather than the board, which results in a drop in capacitive loading and signal-driver size. Other efficiencies include shared resources, such as memories, that reduce the memory-chip count and the number of required controllers.

Key architectural differences arise when designers connect components in a board-level architecture versus an SOC implementation. If an SOC implementation is merely the shrunken version of a board-level implementation, the same bottlenecks arise for either approach. Board-level architectures cannot take advantage of SOC architectural efficiencies. For example, memory-bus bandwidth is often one of the first resources to become unbalanced in a high-frequency, single-core architecture, as processor capacity outstrips the ability of the system bus to stream data to the processor. By its integrated nature, an SOC device enables more granular control of resources, but the architecture must exploit this granularity to increase performance and power efficiency.

Consider a multiprocessor system using several discrete chips, in which each processor can access memory and I/O through the appropriate bridges (**Figure 2a**). A direct SOC implementation of the board-level architecture looks almost identical, with the system bus becoming an internal chip bus (**Figure 2b**). The internal bridge significantly reduces bus latencies. Even though the overall interconnect infrastructure is in a different medium, the components are still logically independent, and they fail to take full advantage of substrate characteristics. For example, when running a bus between chips, minimizing the bus width is a key design consideration to manage pin count, ease the trace layout, reduce the required board space, and lower the overall power consumption. When the interconnect is on a substrate, keeping buses narrow becomes less important. As a consequence, using the same-width bus on an SOC as a board-level implementation unnecessarily constrains the system. Therefore, it is essential to rebuild an SOC instead of mapping components directly from a board-level implementation. You need to rebalance all interconnects, shared resources, and their controllers.

Integration enables greater systemwide visibility, resulting in a more efficient use of resources. For example, when the memory controller or I/O bridge is on-chip, it has access to the various CPU-system states and can make optimal decisions about how to schedule local and system-level accesses. A new capability that is possible with on-chip integration is a shared L2 cache and memory subsystem for each CPU core that can increase the efficiency of data passing between the cores versus a distributed architecture. A shared cache also eases the maintenance of data coherency.

The heart of a multiprocessor system is the interconnect architecture; it defines how the various resources communicate with each other and, as a consequence, how to manage issues such as contention and coherency. The three primary types of interconnect architectures are bus, ring, and switched. A shared bus connects all resources on a single bus. Rings and switches connect resources on a point-to-point basis. To achieve the lowest overall system power, the system must balance performance and the ability to manage coherency.

The chief advantage of a shared bus is that all transactions are visible to all resources. It provides a broadcast capability for implementing efficient data-coherency mechanisms. For instance, a single bus transaction completes the coherency mechanism because all processor cores, caches, memory controllers, and high-speed I/Os are on the same bus. Employing low-voltage swing techniques and avoiding full-voltage rail swings can also significantly contain bus power.

In contrast, a switch requires less bandwidth between each system component. However, to communicate with all of the other resources, such as for integrated coherency management, a processor must send and resolve multiple bus transactions, increasing overall latency. In a four-core system, for example, one core must send a transaction to each of the other three cores as well as receive an acknowledgment back for a total of six transactions, not including the transactions required to update memory and I/O controllers.

From a software developer's perspective, moving to a multiprocessor architecture introduces a potential increase in software-design complexity when partitioning application processing across several cores. For-

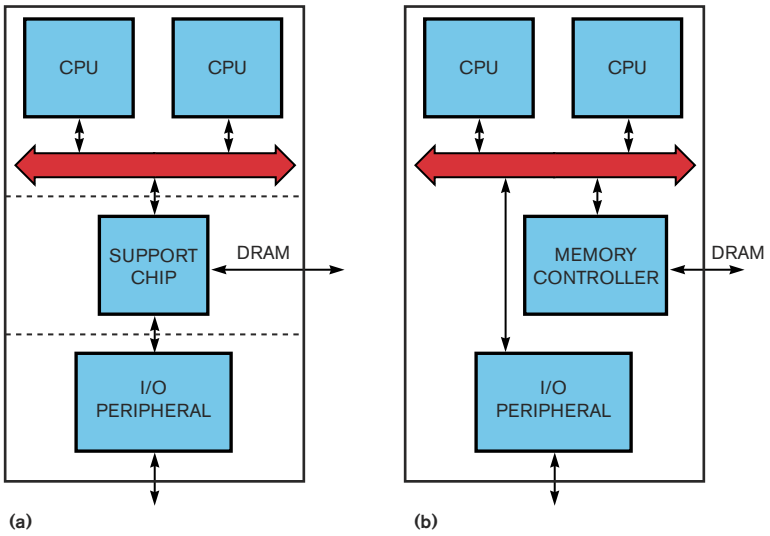

Figure 2 A multiprocessor system built using discrete devices relies upon a system bus to provide access between individual processors and bridges to system resources (a). Implementing this architecture in an SOC carries board-level inefficiencies into the SOC (b).

tunately, many high-performance applications scale in a predictable and symmetrical fashion, such as doubling the number of channels or streams supported in VOIP (voice-over-Internet Protocol) applications or processing 10 times the data in communications applications moving from 100-Mbps to 1-Gbps Ethernet. Developers can still write code in the single-threaded fashion they are accustomed to when developing for a multicore architecture. Developers need to adjust their approach to managing shared resources.

Within single-core, high-frequency architectures, the challenge of accessing resources, such as memory, is more a matter of managing limited bandwidth access when the architecture is unbalanced for an application. With the wider internal interconnect of multiprocessor SOCs, bandwidth imbalance is no longer an issue. Rather, the challenge shifts to managing access and contention for shared resources. For example, when one CPU core operates on a block of data, it may modify the data but delay writing the modification back to memory. If another CPU core tries to use the data, the value may be invalid. Memory-coherency mechanisms prevent this situation, either by supplying the modified value or by locking the data until the first CPU core has written and released modifications.

When encompassing the SOC architecture itself, the SOC can effectively address management of latency and contention, making contention a relatively transparent issue for developers. Additionally, hardware-managed coherency reduces latency. Software-managed coherency consumes execution cycles, increasing latency and power consumption. Again, in high-performance applications, power and performance are intimately tied together. Increasing performance efficiency by 5% reduces power consumption by 5%.

MANAGING POWER

The first axiom of reducing power is to turn off any component that is not in use. Many processors have mechanisms for placing idle peripherals and system blocks into standby or sleep mode until you need them. However, high-performance applications, such as networking, enterprise storage, high-density computing, and wireless infrastructure, are typically running at near to full usage, so such power-management techniques offer limited savings. The next best way to conserve power, then, is to design code that maximizes performance by taking advantage of the architecture's strengths but does not needlessly throw away power, such as by accessing data in such a way that causes the CPU to wait unnecessarily.

In many cases, multiprocessor devices provide automatic mechanisms for improving performance and power consumption through integrated controllers. For example, data coherency is a problem of sufficient complexity that mechanisms to manage it among CPUs, caches, memory, and I/O must be integral parts of the multiprocessor architecture to be effective and efficient.

Developers should not unintentionally break these mechanisms through inappropriate coding techniques. For example, when porting a system from a single-core to a multicore architecture, managing cache coherency takes a different turn. In a single-core implementation, the CPU must flush the cache to make sure to write all data modifications before sending the data to an I/O port. Flushing the cache is unnecessary in a multicore architecture that supports data coherency. Hard-coding-cache flushes unnecessarily burn bandwidth and power, reduce performance, and increase latency.

Modifications to how an application accesses memory may also yield savings. When accessing memory, instead of making several separate accesses, group multiple accesses together consecutively or by type. Consecutive groupings bring several data that the system typically accesses at the same time within the same physical memory line or bank. The system can read four consecutive 8-bit values with a single 32-bit access if they reside on the same memory word. Within a function, locating data on the same page eliminates paging overhead.

When grouping by type, one approach is to reorder a series of reads and writes, grouping several reads and then several writes at once. This approach avoids unnecessary bus turnaround, which is the latency that converting a bus from a read transaction to a write transaction or vice versa produces, improving overall performance and power.

SOFTWARE-MANAGED COHERENCY CONSUMES EXECUTION CYCLES, INCREASING LATENCY AND POWER CONSUMPTION.

In either case, be wary of leaving grouping entirely up to a memory controller. Some memory controllers enforce "fair access" to memory resources. As a consequence, transactions from multiple CPUs can break up a coordinated memory burst, or grouping, reducing efficiency.

To achieve the most gains from grouping, you must be aware of the application level to avoid creating instances of false sharing in which data groupings actually increase latency. Consider a system flag with an instance for each of four processor cores, during which most of the time only the owning processor accesses its flag. If you allocate the four flags as an array, you allocate them in physically consecutive memory. This situation creates inefficient false sharing in the cache. Caches have several lines of multiple bytes, each of which one memory or I/O-resource CPU owns. When you define the array of flags, you contiguously allocate the flags in memory. In other words, they share the cache line when the system reads them into the cache.

One protocol for managing coherency is MESI (modified, exclusive, shared, invalid). According to MESI, when a processor or another resource wants to write a line of data, it needs to ask for exclusive ownership. In the case of the array of flags, ownership of the cache line ping-pongs between CPUs, even though no actual sharing of data takes place and there is no coherency to manage.

Gaining access to the cache line causes a stall with managed coherency; thus, the transaction takes about as long as if the data weren't in the cache at all. Although this stall is still relatively efficient, you can eliminate it. Over several types of data

and throughout a system, such inefficiency can add up. Additionally, it potentially consumes cache space that you could put to better use, minimizing the efficiency of the cache. Proper profiling and analysis tools can help identify situations in which false and unintentional sharing can occur and eliminate instances in which multiple agents fight unnecessarily for the same cache line.

The alternative to array allocation, in this case, is to define the processor flags in a record. Instead of grouping together each set of four corresponding flags, record allocation-group flags by the processor they belong to. Because the consecutive flags belong to the same processor, ownership of the cache line remains stable.

Another way to improve cache and memory performance is to allocate data that a function uses exclusively apart from data that other functions use, especially when a function is working with a lot of data that writes and reads continuously. Clearly differentiating local and global data avoids another form of false sharing and can achieve more efficient bursts that minimize requests for exclusivity and bus turnarounds.

Prefetching can also improve cache efficiency. For example, when streaming in a packet, arrange to allocate a header directly to the L2 cache for immediate use by the I/O port that owns the cache line. The payload, which the CPU needs to touch only once, can bypass the cache, thereby not unnecessarily pushing still-useful data from the cache. Carefully controlling what can enter the cache improves cache efficiency. Again, maximizing performance improves power consumption. Efficient memory and cache usage results in direct performance and power savings.

HARDWARE ACCELERATION

Certain operations suit hardware acceleration. Moving their implementation into hardware through a configurable acceleration engine both improves performance and lowers power consumption by offloading the main CPU core. Consider checksum computations, which are integral parts of many data-integrity mechanisms, because they provide a level of confidence that received data is not corrupt. You must calculate the checksum immediately upon receipt of data; it serves little purpose to burn cycles processing data that you must discard because you later discover it has errors. Additionally, retransmission mechanisms can react more quickly, such as by triggering a resend, the sooner you confirm data corruption.

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With a hardware-checksum engine in place, you can directly place received data in internal or external memory using DMA, depending on how and when you will see the data. In this way, there is no impact on the CPU, and data is ready to load when the CPU requests it. However, if you must verify the checksum, data must pass through the CPU. After you place the data in memory, the CPU must perform an additional memory read and then use the data in the checksum operation. Alternatively, the memory controller can use DMA to place the data directly into the cache, speeding the load operation. However, the CPU must now store the result in memory, so there is a persistent copy, thereby consuming an extra checksum cycle.

With a programmable checksum engine, the checksum of incoming data can process independently of any CPU. In this way, the checksum operation and load or store cycle occur in parallel, decreasing processing latency. Additionally, the checksum engine consumes less power than if a CPU handles it. Finally, by avoiding the CPU, the data does not flush more pertinent data from the cache.

Ideally, an acceleration engine is itself somewhat general-purpose, enabling the same engine that can compute a checksum to calculate a CRC (cyclic redundancy check) or create XOR signatures for RAID (redundant-array-of-independent-disk) applications. Additionally, although a function such as a CRC is a fixed algorithm within an application, the engine should support a configurable element to identify implementations of the function. For example, if an external TOE (TCP/IP offload engine) is in use, you must turn off the CRC engine on either the processor or the TOE. If the engine, such as an inline TOE, is outside the processor, it must be able to queue multiple data streams for multiple CPUs.

CLEARLY DIFFERENTIATING LOCAL AND GLOBAL DATA AVOIDS FALSE SHARING AND CAN MINIMIZE REQUESTS FOR EXCLUSIVITY AND BUS TURNAROUNDS.

The key to sharing resources is to avoid synchronization. Excessive synchronization overhead is one factor that has prevented designers from more quickly adopting multiprocessor implementations. Consider two CPUs sharing an Ethernet MAC (media-access controller). Typically, the status register clears itself when the CPU reads it. Therefore, the first CPU to read the status knows what's happening, but the other CPUs don't. Alternatively, manually clearing the MAC status register introduces the challenge of knowing when all the CPUs interested in seeing the status have had a chance to read it, so that one of them can clear it. Other problems include adding to the output queue and synchronizing with other CPUs to determine the current end of the queue.

Synchronizing CPUs to resolve these issues could consume many cycles and add significant complexity to a simple I/O transaction. SOCs efficiently split a single resource between multiple CPUs and avoid contention in two ways. An integrated controller that manages separate queues and interrupts for each CPU gives each CPU independent control of its own data streams, and the controller resolves all synchronization. Software configurability enables each CPU to flag priority or special-case transactions. The controller can also optimize transactions, such as grouping multiple contiguous transactions, to share the resource in intelligent ways that an external controller cannot. The controller differentiates incoming traffic and routes it to the proper CPU.

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Second, you can modify the I/O port on an SOC to support multiple CPUs. For example, a MAC could offer multiple status registers, one for each CPU. By providing controls for each CPU, the CPUs need not consult each other to use the resource.

Another means of improving performance and power usage is through interrupt steering. For example, data coming from an I/O port often splits between multiple CPUs. If one CPU owns the I/O, when data arrives for another CPU, an interrupt for the I/O occurs, which the owning CPU must relay to the correct CPU. Such relaying adds latency and reduces the determinism of the CPU.

Hardware-based interrupt steering issues an interrupt directly to the correct CPU. Efficient steering becomes important when multiple CPUs want to access the same resource. For example, you could dedicate one CPU to managing all incoming packets from an I/O port and bearing the entire load of evaluating which CPU should receive which packets. Alternatively, steering hardware could direct packets based on a fairness schedule to a particular CPU.

Power limits performance in high-performance architectures, and, accordingly, you can no longer achieve the performance required to support the increasing complexity of multifunction devices simply by throwing additional megahertz at the problem. To address issues of escalating power consumption, engineers need to turn to multiprocessor-SOC architectures that integrate memory and I/O for efficiently sharing resources on a single die. Internal mechanisms for managing coherency and contention remove much of the complexity of multiprocessor design, and, with an understanding of multiprocessor architectures, developers can port their single-core code to work with these mechanisms to maximize performance and minimize power consumption. EDN

AUTHORS' BIOGRAPHIES

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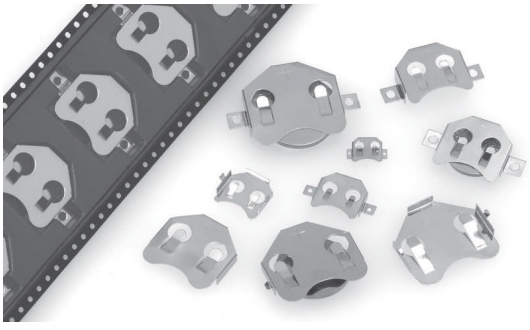

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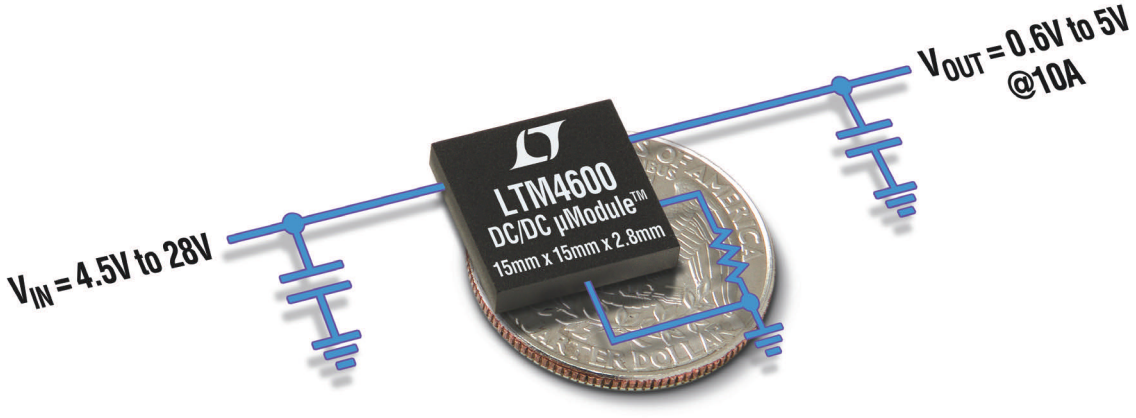

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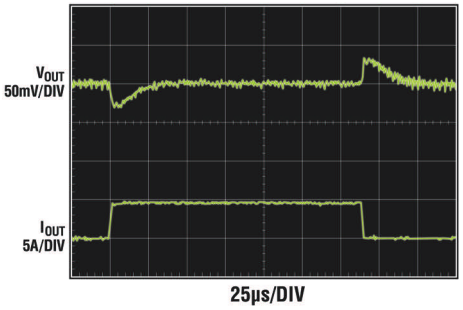

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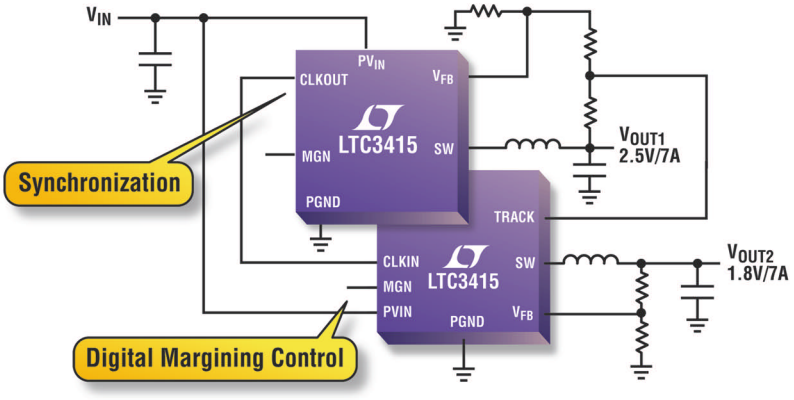

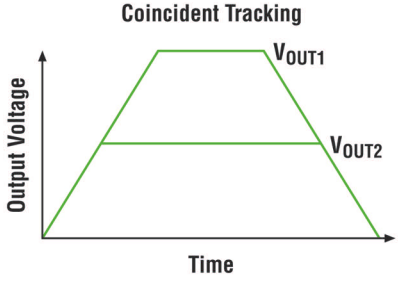

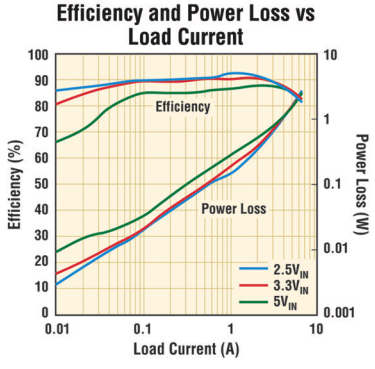

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designideas

READERS SOLVE DESIGN PROBLEMS

CPLD automatically powers itself off

Rafael Camarota, Altera Corp, San Jose, CA

Most of today's CPLDs (complex programmable-logic devices) feature reduced-power operating modes, but, when the system is not in use, a complete shutdown that conserves battery power remains the ultimate power-reduction goal of many designers. **Figure 1** shows how you can add a few discrete components to a CPLD—in this example, an Altera EPM570-T100—to implement a battery-powered system's power-down circuit. An external P-channel MOSFET, Q_1, an International Rectifier (www.irf.com) IRLML6302 or equivalent, serves as a power-control switch for the CPLD, IC_1, and other components in the system. The CPLD and an array of switches control the MOSFET's gate, applying bias that switches on Q_1 whenever a user presses a switch. The CPLD includes an embedded timer that monitors switches and system activity. After a specified period of inactivity, the timer disables the MOSFET's gate drive, powering down the CPLD and other components connected to the MOSFET.

Q_1's source connects to the battery's positive terminal, and its drain connects to IC_1's $V_{CC(INT)}$, $V_{CC(IO1)}$, and $V_{CC(IO2)}$ power pins and other components that require power-down control. When power switches off, a 1-kΩ pullup resistor, R_3, keeps Q_1 off by maintaining its gate at a gate-to-source voltage of 0V. When you turn off IC_1, it presents a leakage path to ground through the CPLD's power-down pin. The EPM570-T100 includes hot-socket protection that limits the current available from any user-accessible device-I/O pin to less than 300 µA. Thus, even in the worst case, the voltage that the I/O pin develops across R_3 doesn't reach the FET's minimum gate-threshold turn-on voltage of 0.7V.

Pressing any switch creates a current path through the switch's contacts and its associated diode, which in turn develops approximately 2.3V of gate-source bias across R_3—more than enough to turn on Q_1 and to power up IC_1 in approximately 100 µsec. When you actuate the mechanical switches, they exhibit a minimum on-time of at least 3 msec, whereas a typical human operator's minimum press-and-release operation consumes at least 30 msec. During these relatively slow response times, the CPLD can turn on, resetting its internal circuitry and asserting its power-down pin to a logic zero that turns on Q_1 before the operator can release the switch.

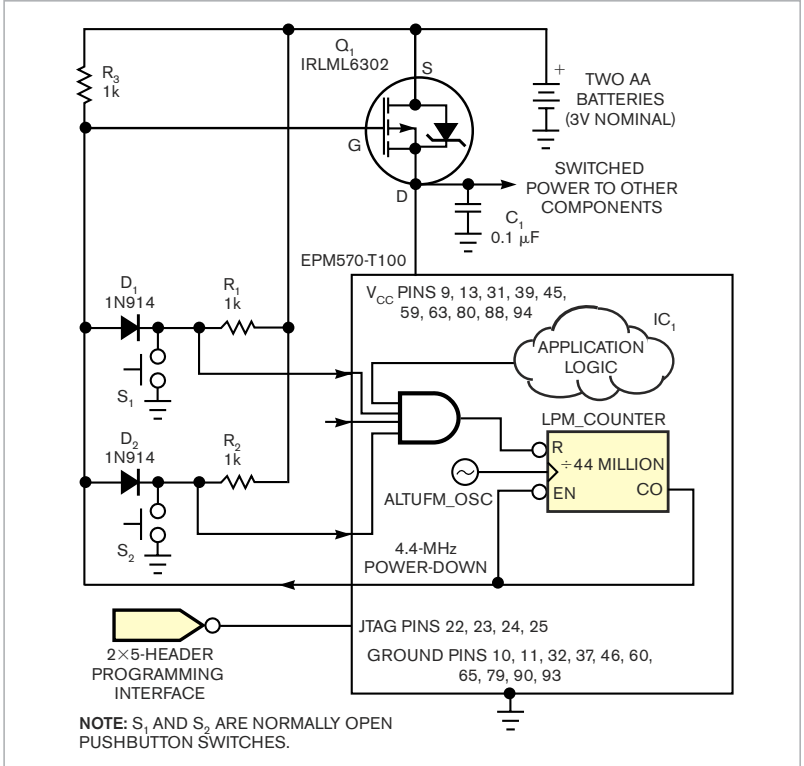

Figure 1 A few external components and internal logic blocks enable a CPLD circuit to switch itself off after a predetermined interval.

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In addition to user-specified application logic (not shown), the CPLD's power-control logic adds a pair of standard parameterized, library-macro circuits that Altera's (www.altera.com) Quartus II development tools generate. An internal 4.4-MHz±25% oscillator, Altufm_osc, drives a modulo-44-million LPM (library-parameterized-module) counter. A logic-low signal that the CPLD's application logic produces or closing any switch resets the counter. When you reset the counter, its carry-out signal goes low and drives the external power-down pin. An inverted version of the carry-out signal re-enables the LPM counter once you remove the reset.

If you leave all switches open and the application logic becomes inactive, the counter counts to 44 million in approximately 10 sec, and the internal carry-out signal goes high, disabling the counter and holding the carry-out signal high. In turn, the power-down pin rises toward V_{CC}, turning off Q_1 when the voltage on the power-down pin reaches 2.3V. Removing power from the CPLD places the power-down pin in the tristate, or disconnected, mode, and R_3 keeps Q_1 off.

You can use JTAG-compliant commands to configure the EPM570-T100 with a download cable you connect to a manufacturer-defined 10-pin header. The process requires that you press an external switch before, during, and shortly after configuration to ensure that the CPLD receives power throughout the configuration process. You can set the inactivity time-out to any desired value by changing the counter's modulus. Although power, ground, and JTAG signals use specific device pins, you can assign any general-purpose CPLD I/O pins as inputs for switches and as the power-down output.

If your application requires a matrix of pushbutton switches, you can use only n diodes to configure an n×m switch matrix for efficient power-up detection (**Figure 2**). In this example, rows of switches connect to the MOSFET's gate through diodes D_1 through D_4. Resistors R_8 through R_{11} provide a ground path for each column of switches and carry current only during key closures, holding the column inputs low while waiting to minimize power-supply current drain.

When a user presses any switch, Q_1's gate goes low, turning on the CPLD. A fast CPLD-power-up routine allows the application to scan the switch matrix's rows and columns and determine which switch a user pressed before the user can release the switch. In this application, the row signals reset the LPM counter's inactivity timer. EDN

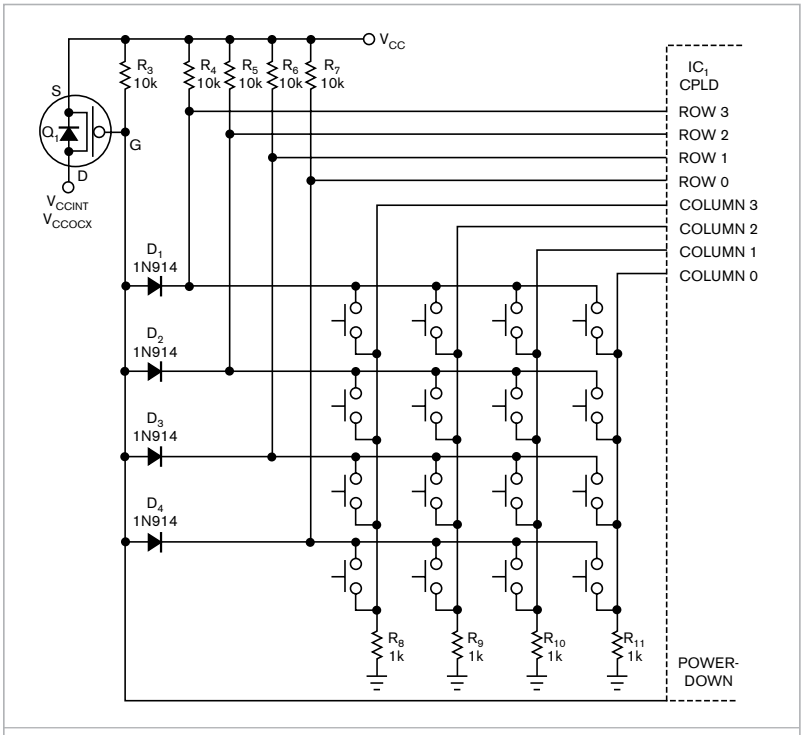

Figure 2 A keypad matrix expands the CPLD circuit's control capabilities and retains the circuit's automatic power-off function.

Amplifier removes common-mode noise on RGB differential-video-transmission line

Tamara Papalias and Mike Wong, Intersil Corp

Comprising four twisted pairs within a durable external sheath, Category 5 network cable offers a common and cost-effective choice for transmitting component-video signals. Three of the pairs can carry RGB video signals, and the fourth pair carries audio, synchronization, and other transmissions. Unfortunately, Category 5 cable lacks shielding, and thus it's somewhat vulnerable to common-mode coupling that induces equal voltages in each of the cable's conductors. As a first line of defense against common-mode problems, you can configure RGB signals as differential voltages, but any voltage difference between the ground references of the twisted-pairs' drivers and receivers results in a common-mode signal on each of the received lines.

Common-mode-noise voltages limit transmission quality of video signals. This Design Idea shows how you can use a single operational amplifier to

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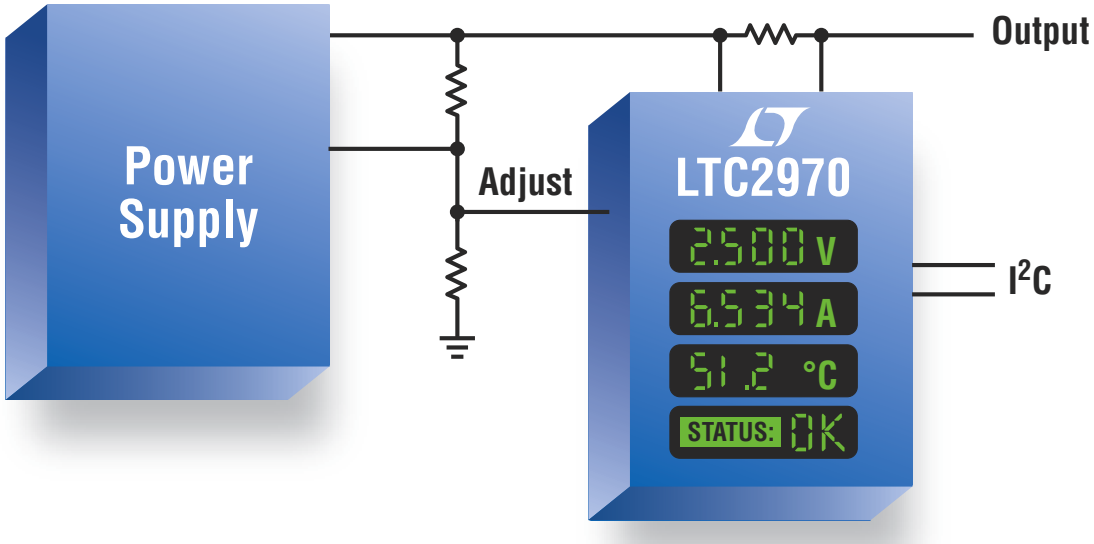

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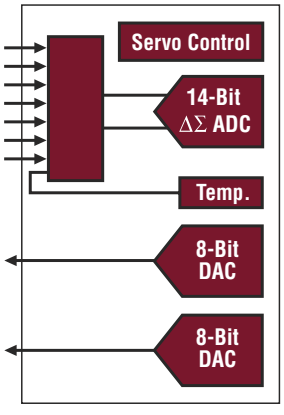

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minimize common-mode signals' effects on differential-component-video receivers. In **Figure 1**, the receiver circuits' ground terminals (in red) show that the ground-reference voltages of each of the RGB differential signals differ from those present at the drivers. To maintain signal quality and minimize reflections, each video-signal twisted-pair transmission line terminates in 100Ω. For example, resistors R_{35} and R_{37} terminate the R+ line, and R_{36} and R_{38} terminate the R− line. Meanwhile, the G and B termination circuits are identical. Any common-mode voltage on the R-signal pair appears at the junction of R_{37} and R_{38} and across R_{39}.

To create a common-mode cancellation voltage, operational amplifier IC_1 sums and inverts the signals on all three or four signal-line pairs. For example, adding the R+ and R− signals cancels their differential-voltage components and doubles the common-mode voltage that each line contributes. Capacitors C_1 and C_2 provide ac coupling for the circuit's input and output, respectively. The output from IC_1 applies a common-mode bias voltage through a matched pair of 30-kΩ resistors, R_{42} and R_{43}, to the R+ and R− receiver network. Close tolerances for R_{42} and R_{43} ensure that the differential voltages delivered at R_{OUT+} and R_{OUT-} closely balance with respect to the inputs' common-mode

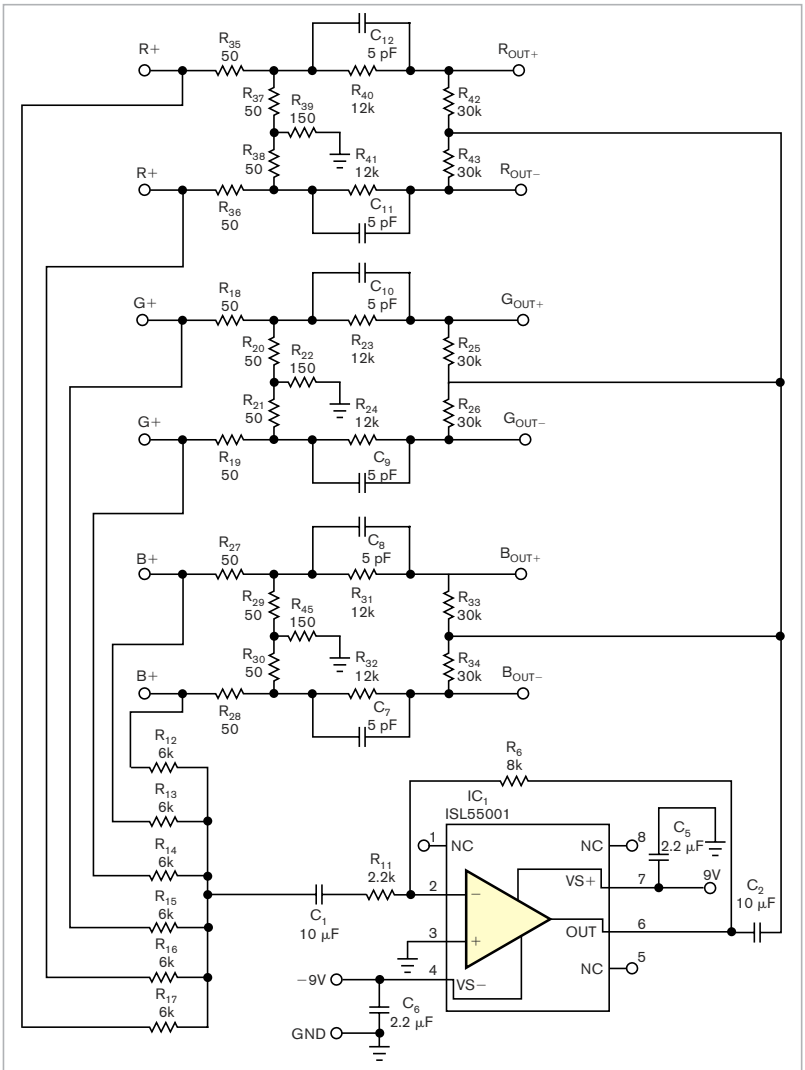

Figure 1 A common-mode-cleanup circuit reduces noise pickup on unshielded Category 5 differential-video signals.

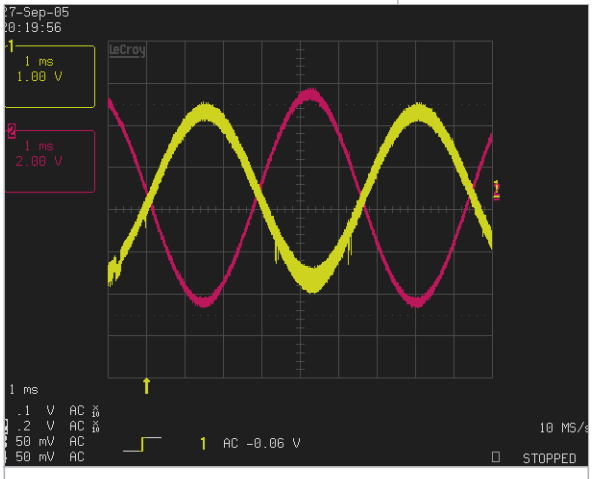

Figure 2 The common-mode signal (yellow trace) heavily influences the video signal (pink trace).

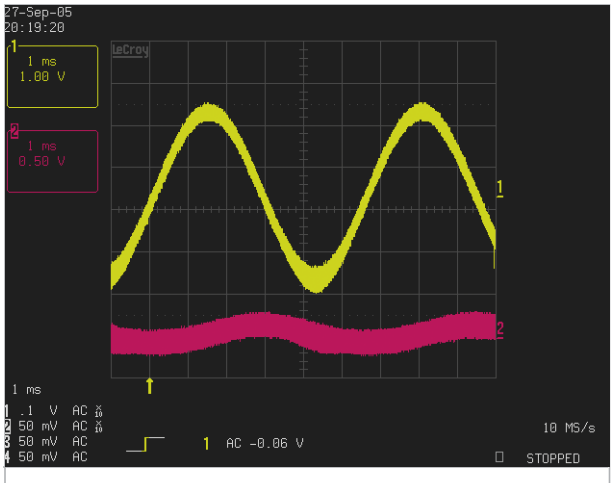

Figure 3 Adding the common-mode-reduction circuit in Figure 1 significantly reduces the amount of common-mode voltage on the video signal.

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voltage. Capacitors C_{11} and C_{12} provide equalization to boost the differential-video signal's higher frequency components.

Before applying cancellation, the signals at the circuit's outputs R_{OUT+} and R_{OUT-} would appear as: $R_{OUT+}=V_{DIFF}/2+V_{CM}$, and $R_{OUT-}=-V_{DIFF}/2+V_{CM}$, where V_{DIFF} represents the desired differential signal, and V_{CM} exists with respect to the circuit's local ground. After applying cancellation, the output signals appear as: $R_{OUT+}=+V_{DIFF}/2+V_{CM}-V_{CMS}=+V_{DIFF}/2$, and $R_{OUT}-=-V_{DIFF}/2+V_{CM}-V_{CMS}=-V_{DIF}/2$, where V_{CMS} represents the summed and inverted common-mode voltage at IC_1's output.

Figure 2 shows a representative 1V peak received signal that's on the R+ line (yellow trace) and an accompanying 2V peak common-mode signal (pink trace). **Figure 3** shows the circuit's common-mode-cancellation abilities. Although the differential signal (yellow) remains unchanged, the common-mode signal (pink) exhibits an 80%, 14-dB reduction. Any mismatch between the time delay and the summed analog signal, which the passive input network and IC_1, respectively, produce, prevents complete cancellation. Also, for best performance, the common-mode signal must not exceed IC_1's common-mode input-voltage rating. In addition, IC_1, an Intersil ISL55001, must exhibit unity-gain stability over a wide bandwidth and an excellent slew-rate response and, for best results, must operate at relatively high-power-supply voltages for good linearity. Use 10-µF, nonpolarized input- and output-coupling capacitors to accommodate extremely low-frequency common-mode voltages. Ensure adequate bypassing for IC_1's power-supply terminals for all frequencies of interest. EDN

Use a switching-regulator controller to generate fast pulses

Mitchell Lee, Linear Technology Corp

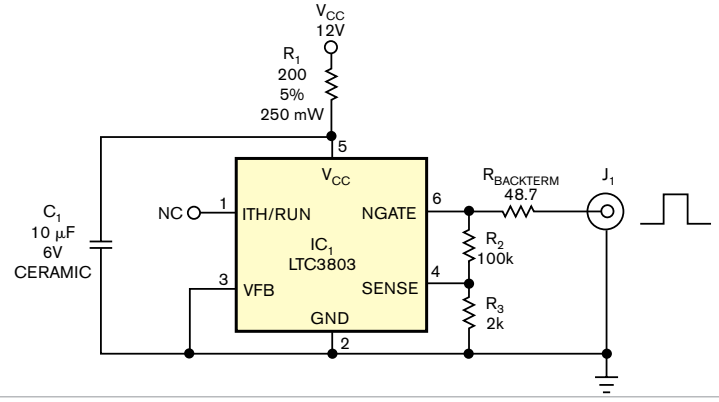

Figure 1 Switching-regulator-controller IC_1 delivers pulses with 1.5-nsec rise and fall times into a 50Ω load.

A source of pulses with fast-rising edges that approximate the step function can help you perform many useful laboratory measurements, including characterization of coaxial cables' rise times and location of cable faults using time-domain-reflectometry methods. For example, evaluating the rise time of a 10- to 20-ft-long RG-58/U cable requires edge-transition times of 1 to 2 nsec. Agilent's (www.agilent.com) HP8012B, a workhorse pulse generator that finds use in many electronics labs, can deliver pulses with rise times of 5 nsec that are adequate for many applications but not for cable characterization.

As an alternative, switching-regulator-controller ICs can deliver gate-drive pulses with rise and fall times of less than 2 nsec, making them ideal candidates for laboratory pulse-generation service. A simple implementation uses Linear Technology's (www.linear.com) LTC3803 constant-frequency flyback controller, IC_1 (**Figure 1**). The controller self-clocks at 200 kHz, and applying a sample of its output to its Sense pin causes the controller to operate at its minimum duty cycle and produce a 300-nsec-wide output pulse.

The LTC3803's output can deliver more than 180 mA into a 50Ω load, so use a low-series-inductance bypass capacitor that connects as directly as possible between IC_1's power and ground (pins 5 and 2). The decoupling components, C_1, a 10-µF ceramic capacitor, and R_1, a 200Ω resistor, minimize pulse-top aberrations without introducing amplitude droop. The circuit's output directly drives a 50Ω termination at amplitudes as high as 9V. For applications that require maximum pulse fidelity, use a back-termination resistor, $R_{BACKTERM}$, to suppress triple-transit echos and absorb reflections from the cable and any mismatch in the cable's far-end termination impedance. Back-termination also helps when driving passive filters, which expect to see a specific generator impedance. The LTC3803's output impedance is approximately 1.5Ω, which affects the value of the back-termination resistor. The back-termination technique

(continued on pg 106)

LINEAR TECHNOLOGY

DESIGN NOTES

Ideal Diode Controller Eliminates Energy Wasting Diodes in Power OR-ing Applications – Design Note 386

David Laude

Introduction

Many modern electronic devices need a means to automatically switch between power sources when prompted by the insertion or removal of any source. The LTC®4412 simplifies PowerPath™ management and control by providing a low loss, near ideal diode controller function. Any circuit that could otherwise use a diode OR to switch between power sources can benefit from the LTC4412. The forward voltage drop of an LTC4412 ideal diode is far less than that of a conventional diode, and the reverse current leakage can be smaller for the ideal diode as well (see Figure 1). The tiny forward voltage drop reduces power losses and self-heating, resulting in extended battery life. Features include:

- Voltage drop across the controlled external MOSFET of only 20mV (typical)
- Low component count helps keep overall system cost low
- 6-pin ThinSOT™ package permits a compact design solution
- Wide supply operating range of 2.5V to 28V (36V absolute maximum)
- Protection of MOSFET from excessive gate-to-source voltage with VGS limiter
- Low quiescent current of 11µA with a 3.6V supply, independent of the load current
- A status pin that can be used to enable an auxiliary MOSFET power switch or to indicate to a microcontroller that an auxiliary supply, such as a wall adapter, is present
- A control input pin for external control, such as from a microcontroller

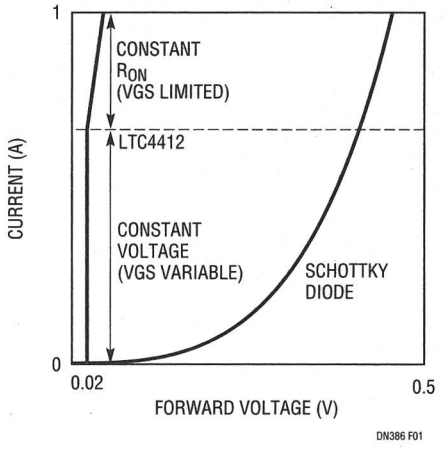

Figure 1. LTC4412 Ideal Diode Controller vs Schottky Diode Characteristics

Applications include anything that takes power from two or more inputs:

- Cellular phones
- Portable computers
- PDAs
- MP3 players and electronic video and still cameras
- USB peripherals
- Wire-ORed multipowered equipment
- Uninterruptible power supplies for alarm and emergency systems
- Systems with standby capabilities
- Systems that use load sharing between two or more batteries
- Multibattery charging from a single charger
- Logic controlled power switches

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Automatic Power Switching Between Two Power Sources

Figure 2 illustrates an application circuit for the automatic switchover of load between two power sources, in this example a wall adapter and a battery. While the wall adapter is absent, the LTC4412 controls the gate of Q1 to regulate the voltage drop across the MOSFET to 20mV, thus wasting negligible battery power. The STAT pin is an open circuit while the battery provides power. When a wall adapter or other supply connected to the auxiliary input is applied, the SENSE pin voltage rises. As the SENSE pin voltage rises above V_{IN} – 20mV, the LTC4412 pulls the GATE voltage up to turn off the P-channel MOSFET. When the voltage on SENSE exceeds V_{IN} + 20mV, the STAT pin sinks 10µA of current to indicate that an AC wall adapter is present. The system is now in the reverse turn-off mode, where power to the load is delivered through the external diode and no current is drawn from the battery. The external diode is used to protect the battery against some auxiliary input faults such as a short to ground. Note that the external MOSFET is wired so that the drain to source diode will reverse bias and not deliver current to the battery when a wall adapter input is applied.

Load Sharing

Figure 3 shows a dual battery load sharing application with automatic switchover of power between the batteries and a wall adapter. In this example, the battery with the higher voltage supplies all of the power until it has discharged to the voltage of the other battery. Once both batteries have the same voltage, they share the load with the battery with the higher capacity providing proportionally higher current to the load. In this way, the batteries discharge at a relatively equal rate, maximizing battery run time.

When a wall adapter input is applied, both MOSFETs turn off and no load current is drawn from the batteries. The LTC4412's STAT pins provide information as to which input is supplying the load current. The ganging of the LTC4412s can be applied to as many power inputs as are needed.

Conclusion

The LTC4412 provides a simple means to implement a low loss ideal diode controller that extends battery life and reduces self heating. The low external parts count results in low implementation cost and with its ThinSOT 6-pin package, a compact design as well. Its versatility is useful in a variety of applications (see the LTC4412 data sheet for additional applications).

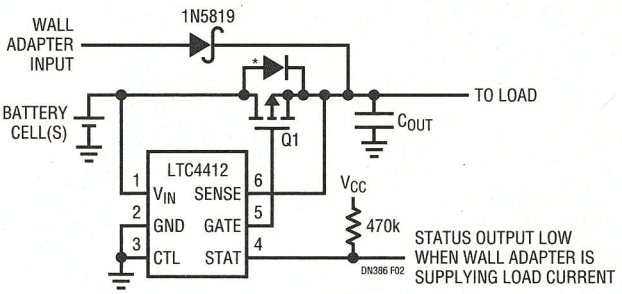

Figure 2. Automatic Power Switching Between a Battery and a Wall Adapter

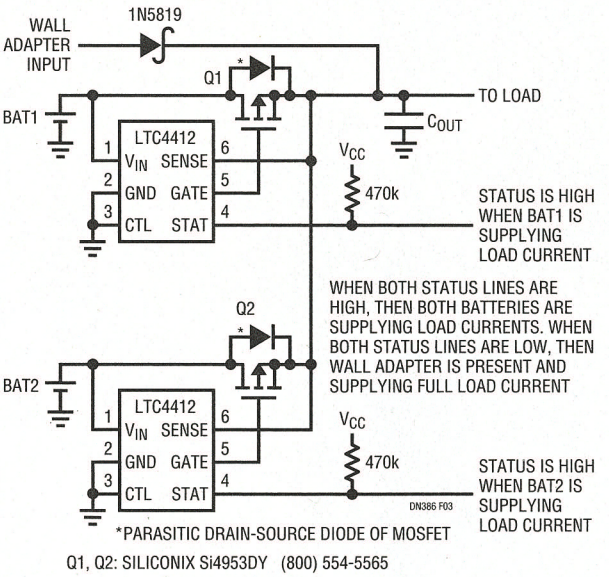

Figure 3. Dual Battery Load Sharing with Automatic Switchover of Power from Batteries to Wall Adapter

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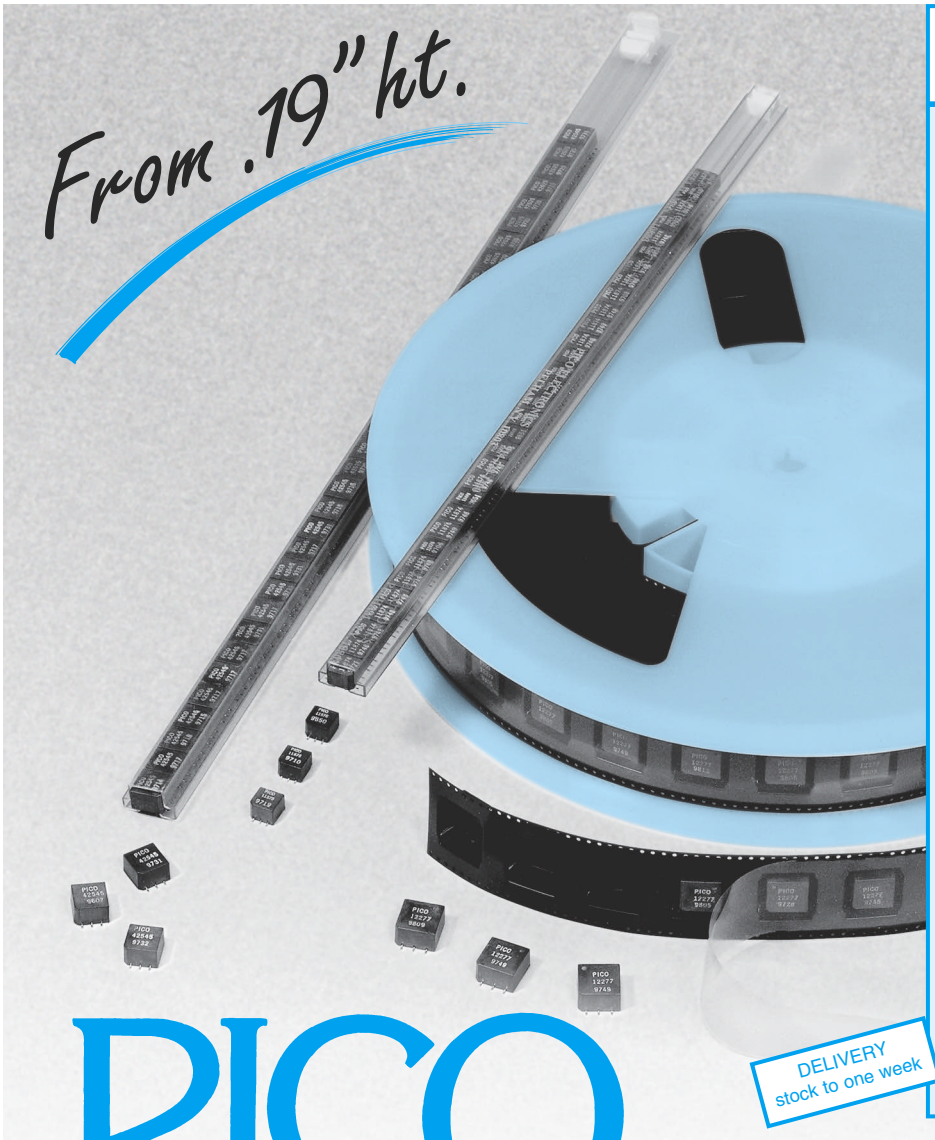

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works well with load impedances of at least 2 kΩ. At impedances higher than that value, parasitic impedances associated with the terminating resistor and IC_1 degrade bandwidth and pulse fidelity.

In a back-terminated, 50Ω system, the circuit delivers a 4.5V output pulse with symmetric rise and fall times of 1.5 nsec, pulse-top-amplitude aberrations of less than 10%, and amplitude droop of less than 5%. Directly driving a 50Ω load doesn't degrade the output's rise and fall times. For best pulse fidelity, use stripline techniques to route IC_1's output directly to the termination resistor and output connector J_1. Using a 100-mil-wide trace on a 1/16-in., double-sided, glass-epoxy pc board approximates a 50Ω surge impedance. EDN

Shift registers and resistors deliver multiphase sine waves

Gary Steinbaugh, 4 E A Transform, Loveland, OH

Sine waves with fixed phase relationships find application in communications equipment, instrumentation, and power sources. Although you can use any of several traditional analog techniques to generate basic sine-wave signals, this Design Idea offers a simple method that uses only digital logic and fixed-value resistors (**Figure 1a**). A common clock pulse drives three of four sections of a pair of CD4015 4-bit shift registers that recirculate a pattern comprising 12 zeros and 12 ones—that is, 000000000000111111111111. Each of the registers' outputs drives a resistor, R_1 through R_{12}, that connects to a summing node. If all of the resistors were of equal value, their summed output would comprise a stepped linear triangular waveform at a repetition frequency one-twenty-fourth that of the clock frequency.

To produce a stepped sinusoidal output waveform, you replace the equal-value resistors with the weighted values in **Figure 1a**. If you use resistors of 1% tolerance, the output's amplitude will approximate that of a true sine wave to better than 1°. To produce a cleaner sine wave, a lowpass filter helps remove clock-pulse feedthrough and stepped-edge transients (**Figure 1b**). For many applications, a simple one-pole lowpass filter/buffer provides adequate filtering, but a more elaborate multipole filter further increases output purity.

You can add a second set of registers and resistors, R_{13} through R_{24}, to produce cosine and sine waves offset by a 90° phase shift—that is, two sine waves in quadrature (**Figure 2**). Register IC_{2A}'s inverted and recirculated output from Q4 generates the 0000000000-00111111111111 bit pattern that the first set of shift registers uses. IC_{2B}'s Q4 output produces the D input that you apply to the second set of shift registers—IC_{2B}, IC_{3A}, and IC_{3B}—which in turn generate a 90° phase-shifted version of the bit pattern to form a cosine wave. The cosine bit pattern requires no recirculation and simply propagates

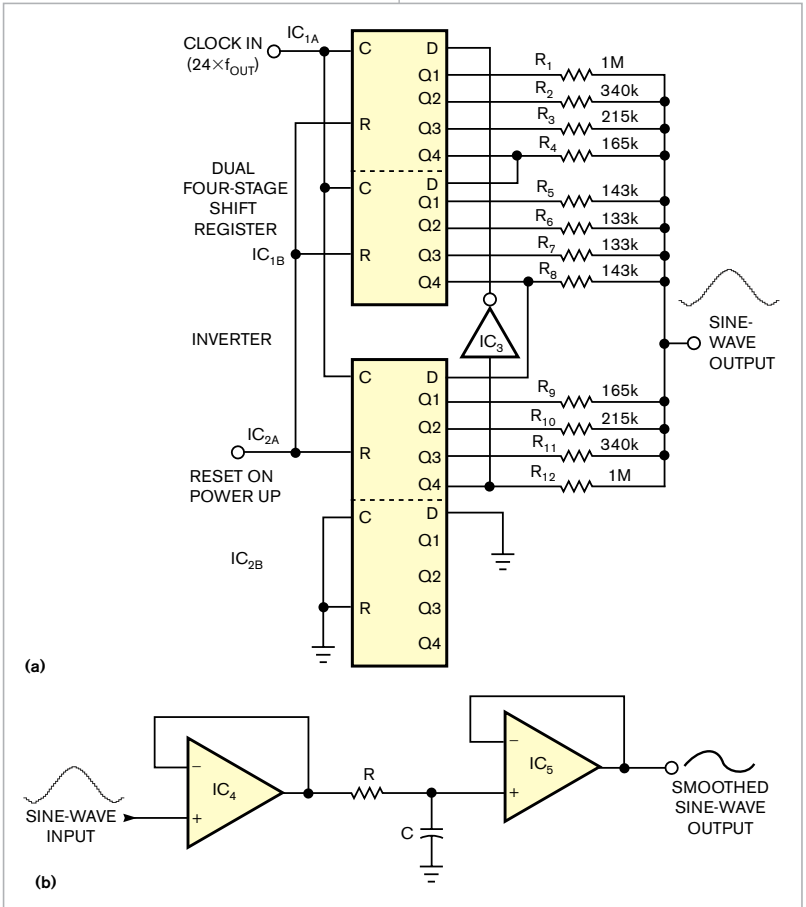

Figure 1 A pair of shift registers, an inverter, and a handful of precision resistors form a sine-wave generator (a). Two operational amplifiers form a resistance-capacitance lowpass filter that removes clock-signal artifacts from the output (b).

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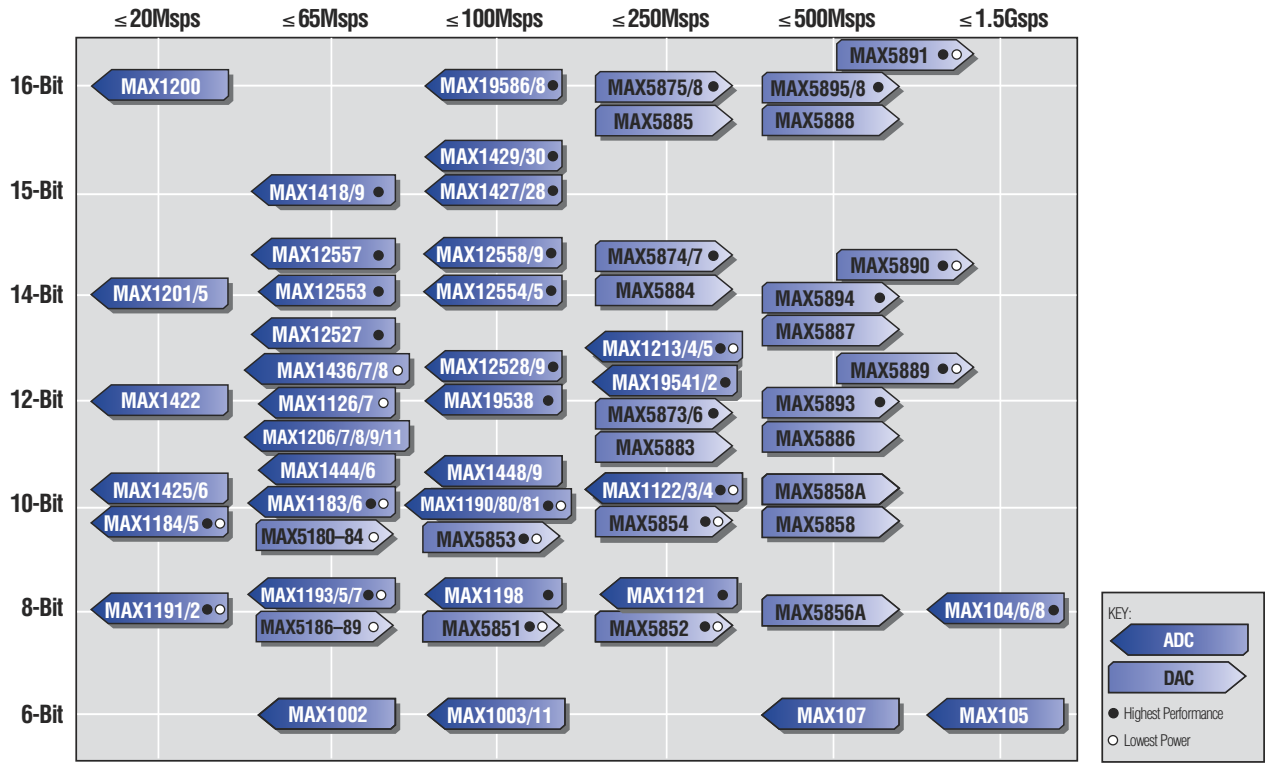

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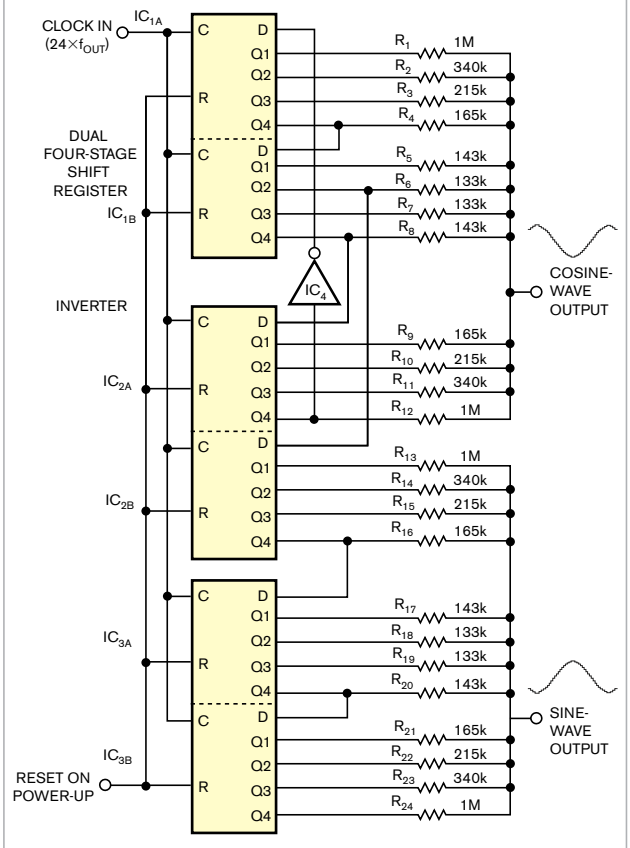

Figure 2 Add a second set of shift registers to generate a cosine wave.

through the second set of shift registers and "falls off the end." To adjust the second output's phase shift with respect to the first output from 15 to 180° in 15° increments, you can connect IC_{2A}'s D input to any one of IC_1's Q outputs.

Figure 3 illustrates a three-phase sine-wave-generator circuit. The Q4 output from IC_{1B} supplies the D input to the second set of shift registers, IC_{2A} and IC_{2B}, to produce the recirculated bit pattern. In similar fashion, the Q4 output from IC_{3A} supplies the D input to the third set of shift registers, IC_{4A}, to transfer a duplicate bit pattern that's phase-shifted by 240° with respect to the output from the first set of shift registers.

Register IC_{2B}'s D input connects to IC_{1B}'s Q4 output to produce a signal—Phase 2's output—that lags behind the Phase 1 output by 120°. In similar fashion, register IC_{4A}'s D input connects to IC_{3A}'s Q4 output to produce a signal—Phase 3's output—that lags behind Phase 2's output by 120°, or 240° with respect to Phase 1.

You can expand the basic circuit to accommodate additional signal phases. The weighted resistors' values are adequate for low-frequency sine waves and 4000-series CMOS-logic devices. However, you can scale the resistors' values to accommodate other output frequencies and logic families. EDN

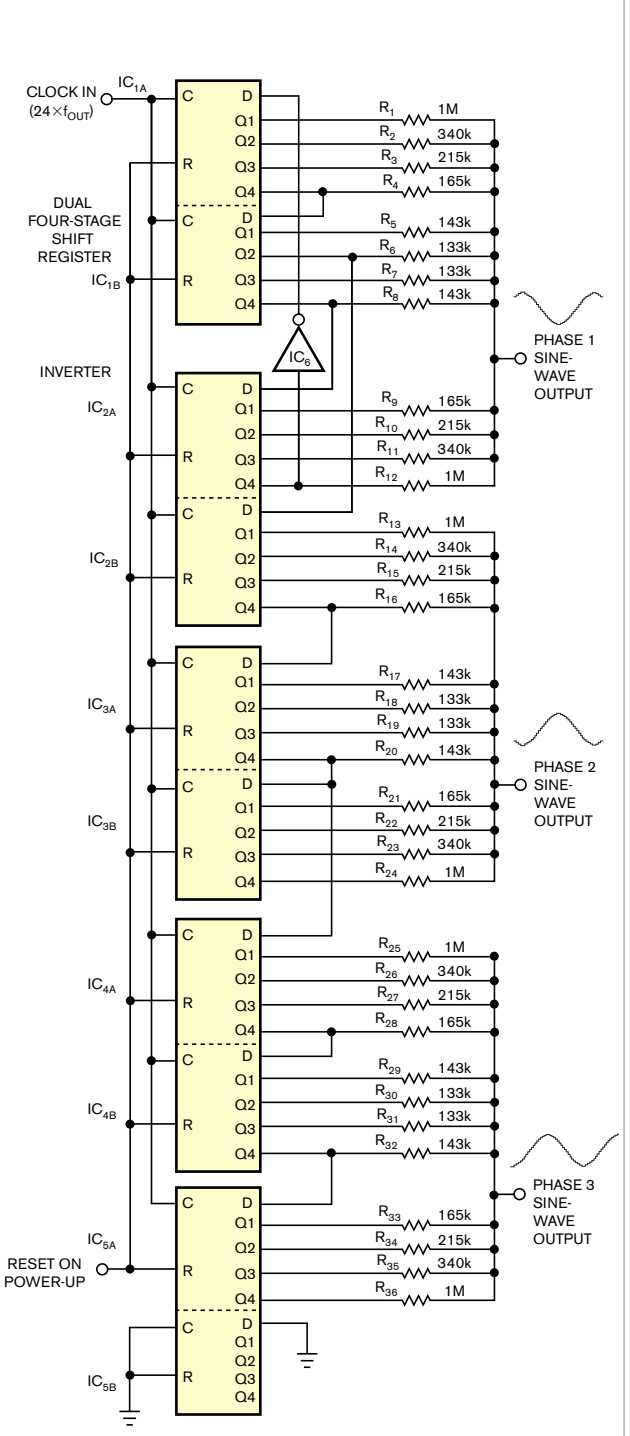

Figure 3 Adding a third set of shift registers yields a three-phase sine-wave output.

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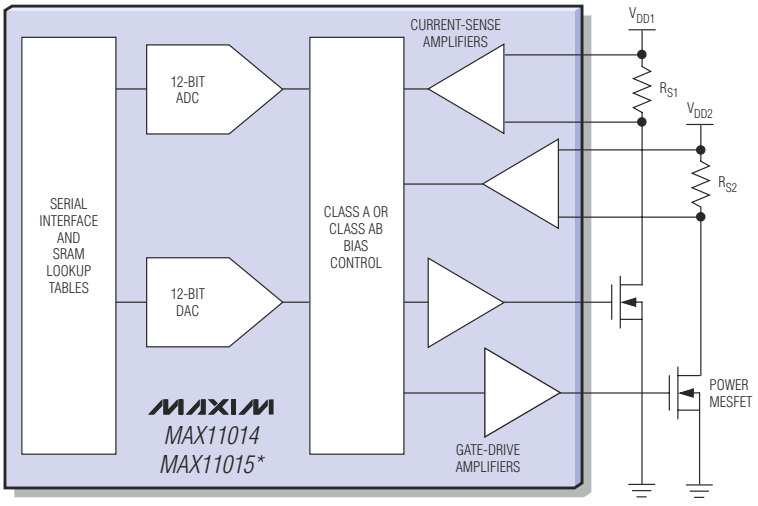

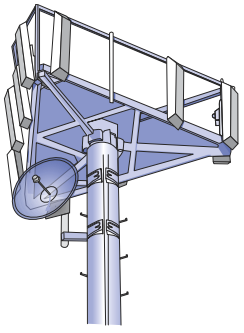

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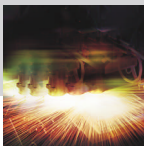

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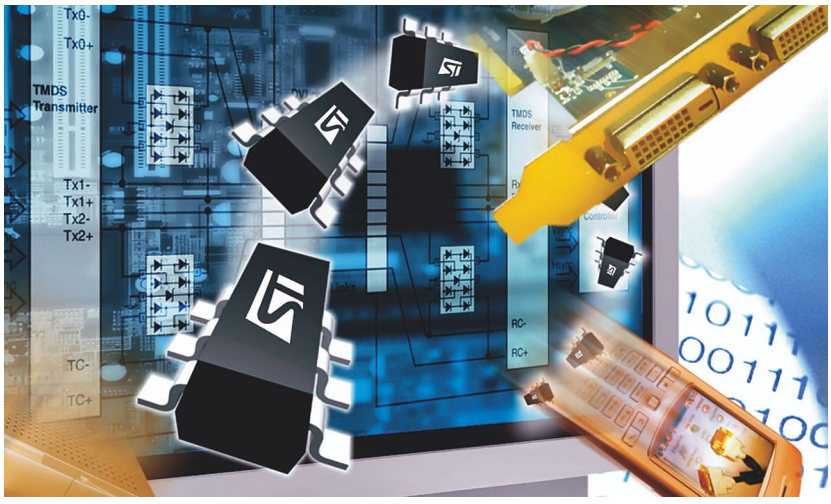

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NexTec, www.nexteklightning.com

LVDS buffer has ESD protection

Featuring an on-chip termination for maximum signal integrity, the 800-Mbps, quad-LVDS (low-voltage-differential-signaling) DS90LV804 buffer has 15 kV of ESD protection. The four-channel buffer delivers LVDS signals across cables and backplanes in electronic systems, suiting it for telecom, datacom, industrial, medical, automotive, and office-imaging applications. Measuring 5×5×80 mm in an LLP-32 package, the DS90LV804 buffer costs $2.95 (1000).

National Semiconductor, www.national.com

EMI-filter arrays integrate ESD-protection diodes

These EMI-filter arrays incorporate ESD-protection diodes, attenuating unwanted signals by 30 dB over the 900-MHz to 2.3-GHz frequency range, with 30 to 100Ω line-resistance values. The devices come in small, leadless, plastic LLP75-6A, LLP75-7A, LLP-

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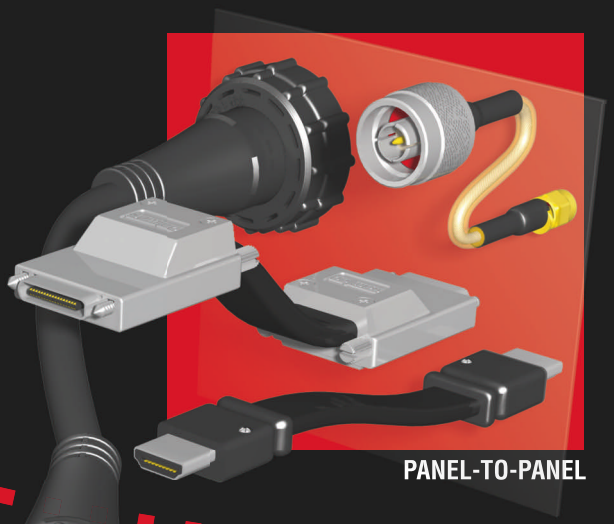
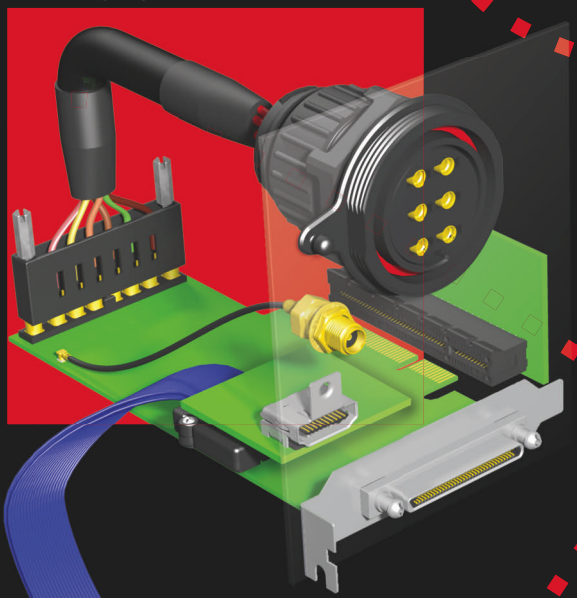
SIGNAL INTEGRITY



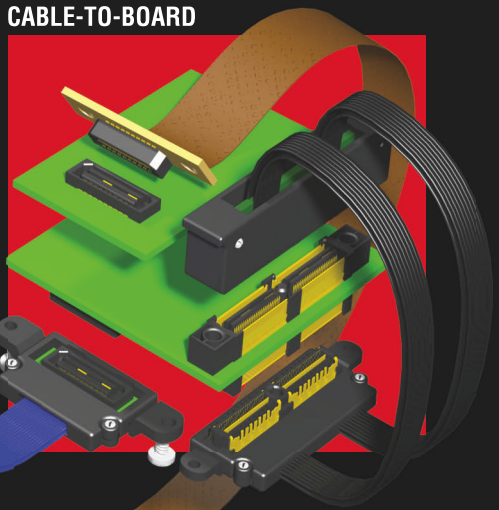
PANEL-TO-PANEL

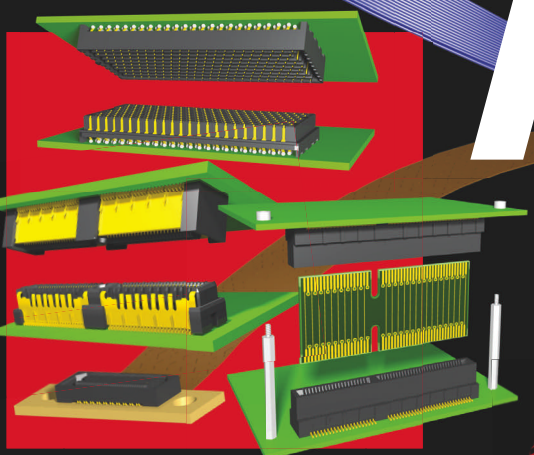
PANEL-TO-BOARD



FROM THE OUTSIDE IN

CABLE-TO-BOARD





BOARD-TO-BOARD

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www.samtec.com/si

productroundup

CIRCUIT PROTECTION

70-9A, and flip-chip BGA packages, providing two-, three-, four-, and six-channel configurations, respectively. Additional features include 30-kV ESD protection and transient protection for data lines. The filter arrays cost 15 to 25 cents (100,000).

Vishay Intertechnology, www.vishay.com

Two-line protection device meets IEC standards

Targeting ADSL and WAN (wide-area-networking) equipment, the two-line secondary Rclamp 7002M protection device has a 10-pF I/O-to-ground capacitance. A 1-kW surge capability allows for shielding of sensitive circuits in central-office or customer-premises equipment from ESD, CDEs (cable-discharge events), EFTs (electrical fast transients), or lightning. The device meets IEC standards for ESD, EFT, and lightning. Connecting to the V_{CC} and the ground to match the system voltage within the range, the product has a 3.3 to 70V range. The Rclamp7002M costs 76 cents (10,000).

Semtech, www.semtech.com

10A relays use low-power-consumption coils

The G5LB and G5LB-25 series of single-pole, power-pc-board relays switch 10A at 120 to 250V ac and 8A at 30V dc and can switch digital signals. Peripherals include a 360-mW power-consumption coil, a 200,000-operation electrical life, and a 19.6×15.6×15.25-mm architecture. G5LB and G5LB-25 relays cost 45 to 63 cents (10,000).

Omron Electronic Components, www.components.omron.com

INTEGRATED CIRCUITS

DVD-recorder chip sets integrate PVR and set-top-box functions

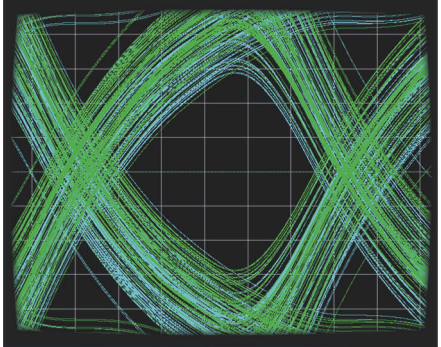
Adding onto the vendor's line of DVD-recorder devices, the Activa 220 and 230 processors include set-top-box functions. The 220 SOC (system-on-chip) features a high-speed IDE interface providing PVR (personal-video-recorder) functions for combination hybrid-optical-disk-drive and hard-disk-drive recorders. An optional dedicated interface to the vendor's HD-Xtreme video processor for HD-JPEG display and HDMI output is also available. The 230 processor integrates two DVB (digital-video-broadcast) transport-processor interfaces with free-to-air support for dual tuners in addition to the 220 optical- and hard-disk-drive features. The Activa 220 and 230 chip sets cost $30 and $35, respectively.

Zoran Corp, www.zoran.com

Single-chip microphone features a PDM output

Based on CMOS MEMS (microelectromechanical-systems) technology, the AKU2000 single-chip microphone integrates an acoustic transducer, an output amplifier, and a fourth-order sigma-delta modulator. For output, the microphone uses a PDM (pulse-density-modulated), single-bit digital-output stream insensitive to RFI and EMI. The device supports a 1- to 4-MHz input-clock frequency, a 2.8 to 3.6V operating

DON'T BLINK



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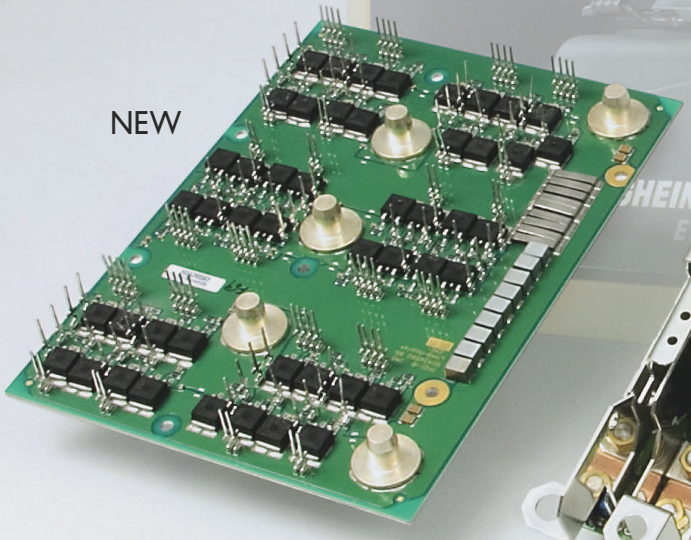
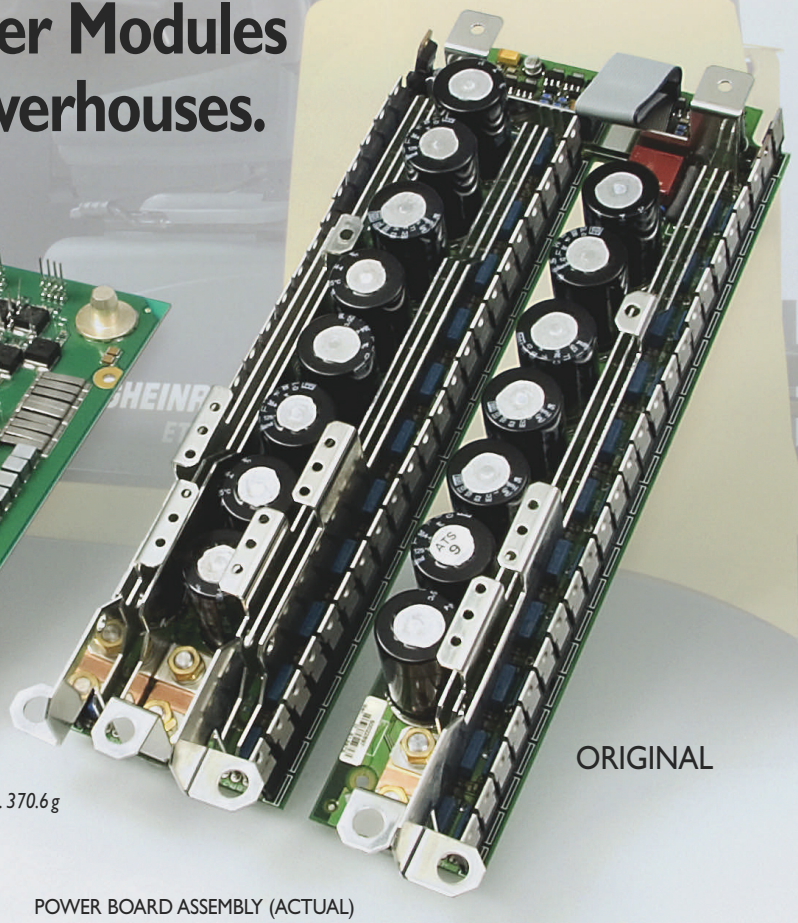


POWER BOARD ASSEMBLY (ACTUAL)
(48) FETs (9) Low profile capacitors (5) Low profile bus bars Total Wt. 370.6 g



ORIGINAL

POWER BOARD ASSEMBLY (ACTUAL)
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productroundup

INTEGRATED CIRCUITS

range, and 750-μA power consumption. In power-down mode, the microphone consumes 75 μA when there is no clock input to the microphone. Available in a 4×4-mm footprint, the AKU2000 costs $3.87 (1000).

Akustica, www.akustica.com

Analog-volume-control IC has 5 and 9V options

The CS3318 analog-volume-control IC provides a 127-dB dynamic range, with a 118-dB adjustable range and negligible distortion. Supporting eight channels of audio, the device operates from a 9V power supply. The pin-compatible CS3308 IC is available in a 5V version. The CS3318 and CS3308 cost $9.22 and $6.97 (10,000), respectively.

Cirrus Logic Inc, www.cirrus.com

USB host features 26-MHz SPI

Featuring a 26-MHz SPI (serial peripheral interface), the MAX-3421E USB host and peripheral controller add USB-host capabilities to any microprocessor. Features include a −40 to +85°C temperature range, a 5×5-mm footprint, and availability in TQFP-32 and TQFN-32 packages.

Maxim Integrated Products, www.maxim-ic.com

Advanced video processor supports DVR and MP3 players

The Sil 8200 advanced video processor features dual video/image-processing pipelines and integrated DVR (digital-video-recorder) and MP3-player support. The device includes a RISC processor, an IDE hard-disk controller supporting DVR functions, MP3/AAC decoders for auto playback, and a JPEG decoder for photo display. Additional features include a built-in analog-video front end for 12 channels of standard-definition television with an advanced 3-D comb filter for high-quality video. The device also has two 24-bit digital-video-input ports supporting 1920×1080-pixel progressive HDTV resolution. The processor handles 12 composite, S-video, and component-video signals. Key features of the RISC microprocessor include a 32-MIPS RISC architecture, a programmable clock from 600 kHz to 166 MHz, and 14 kbytes of cache memory. The video-processor pipelines feature dual-processing paths; 3-D motion-adaptive deinterlacing; 3-D motion-adaptive noise reduction; advanced scaling with moiré cancellation; and image processing, including DCTI, DLTI, full HSB, and contrast controls. The integrated storage and mobile-player interfaces include acceleration for MP3, AAC, WMA, and JPEG decoding; an integrated IDE hard-disk-drive controller for DVR functions; flash-media direct connection; and a USB 1.1 interface, enabling MP3 playback and photo display from digital cameras. Available in a PBGA-388 package, the Sil 8200 costs $20 (10,000).

Silicon Images, www.siliconimages.com

MPEG-video-processor family integrates conditional access

The MPEG-video-processor X-Code 2100 family of digital/analog-video processors uses PCI Express x1 and PCI v2.3 interfaces, allowing compressed and uncompressed video data over the main bus. Series features include single- and dual-stream MPEG2/4 D1 compression at 30 frames/sec, real-time transrating and transcoding, and conditional access with a Smart Card interface for ControlWord exchange. Prices for the XCode 2100 family of chips range from $14 to $30.

ViXS Systems, www.vixs.com

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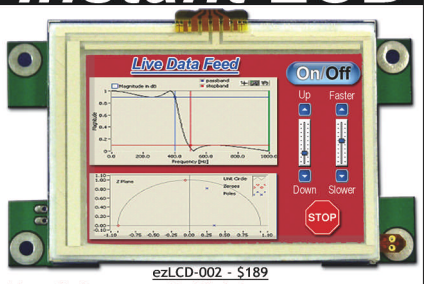

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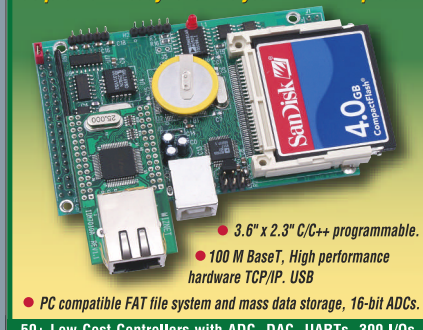

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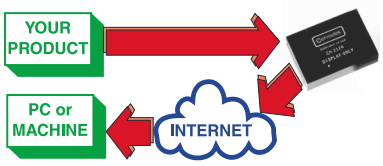

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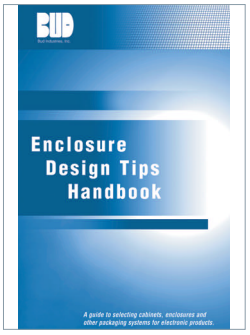

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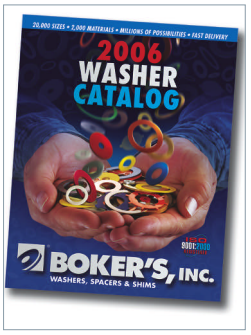

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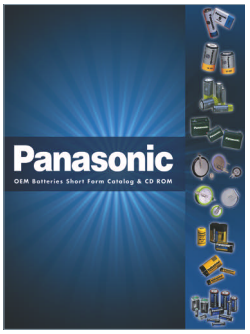

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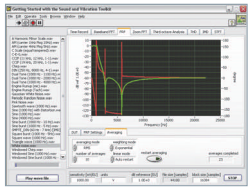

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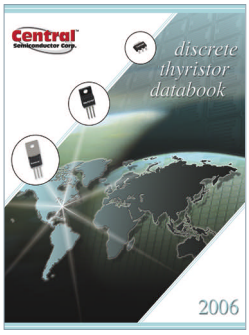

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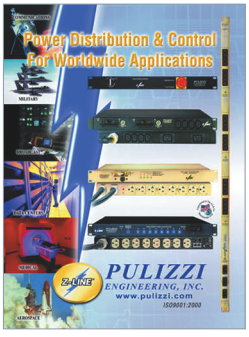

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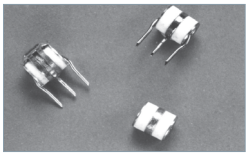

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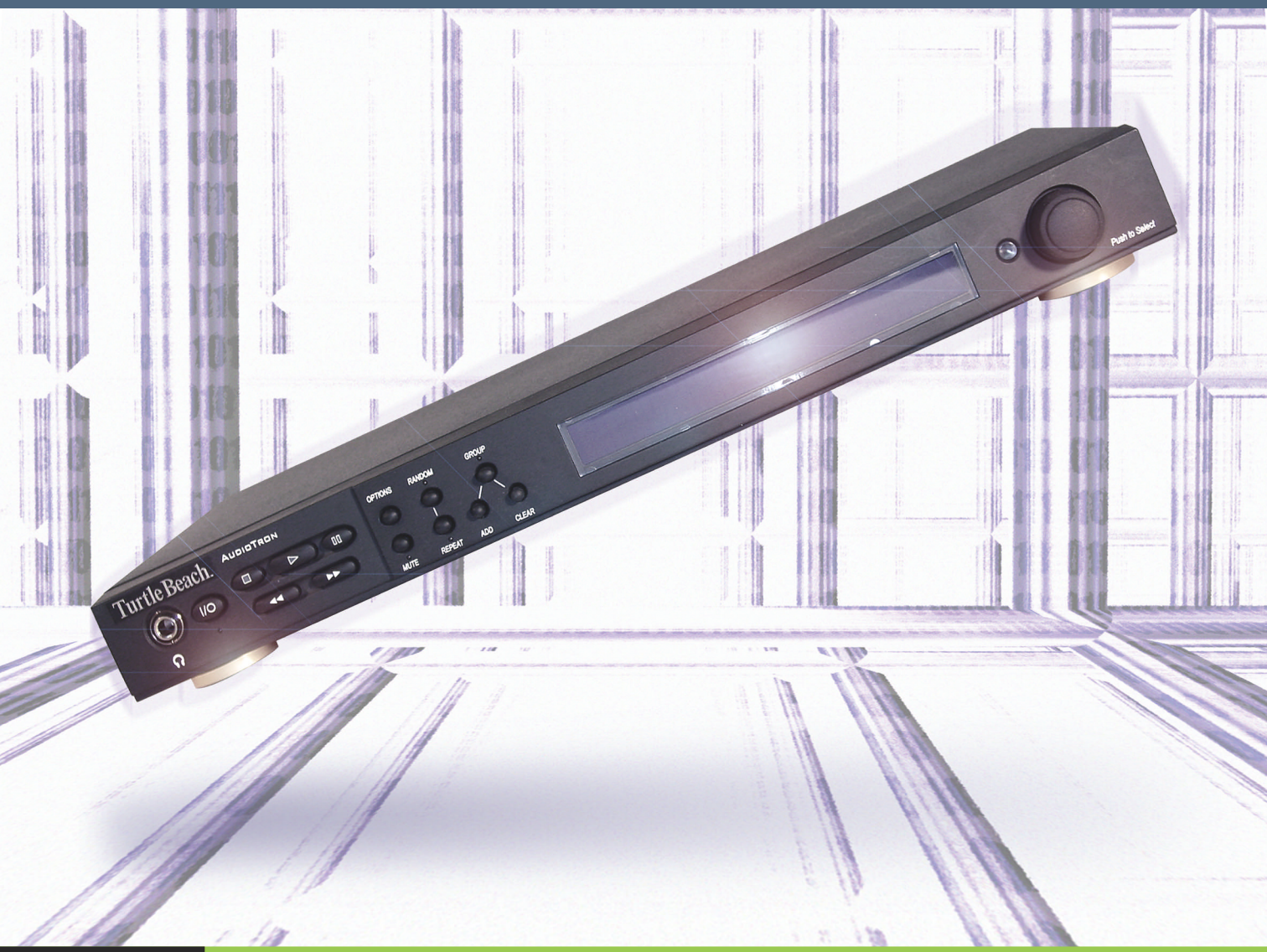

STATS Included Cirrus Logic EP7312; 16 Mbytes of DRAM / Ceased production spring 2004

Audio player tackled search all by itself

At the 2001 Windows Hardware Engineering Conference, Voyetra Turtle Beach unveiled the Audiotron digital-audio network appliance. In some respects, the Audiotron is woefully obsolete compared with today's digital media adapters. It doesn't drive an external display, instead relying on a small, built-in LCD. It doesn't support subscription WMA (Windows Media Audio) content or other modern audio codecs, such as AAC (advanced audio coding)—either with or without the DRM (digital-rights-management) technology that Apple's iTunes uses. It doesn't support playback of still-image or video content, and it lacks built-in Wi-Fi capability and wired Ethernet support beyond 10 Mbps (although early versions *did* support the Home Phoneline Network Alliance).

However, the Audiotron has one ultracool feature. In part because it runs a full Linux operating system, it can proactively search for, find, index, and pull content from any other LAN- or—with a firewall hole—WAN-connected storage device that supports the pervasive SMB (server-message-block) protocol. You don't need to restrict your audio-content-storage options, and, therefore, your audio-content options, by relying on a Mac- or Windows-only server program. Instead, you can stream audio that resides on a diverse set of SMB-cognizant LAN clients, such as Macs, Windows PCs, Linux-server appliances, and a variety of NAS (network-attached-storage) boxes—all without installing any server-side software on each machine. That's slick.—by Brian Dipert

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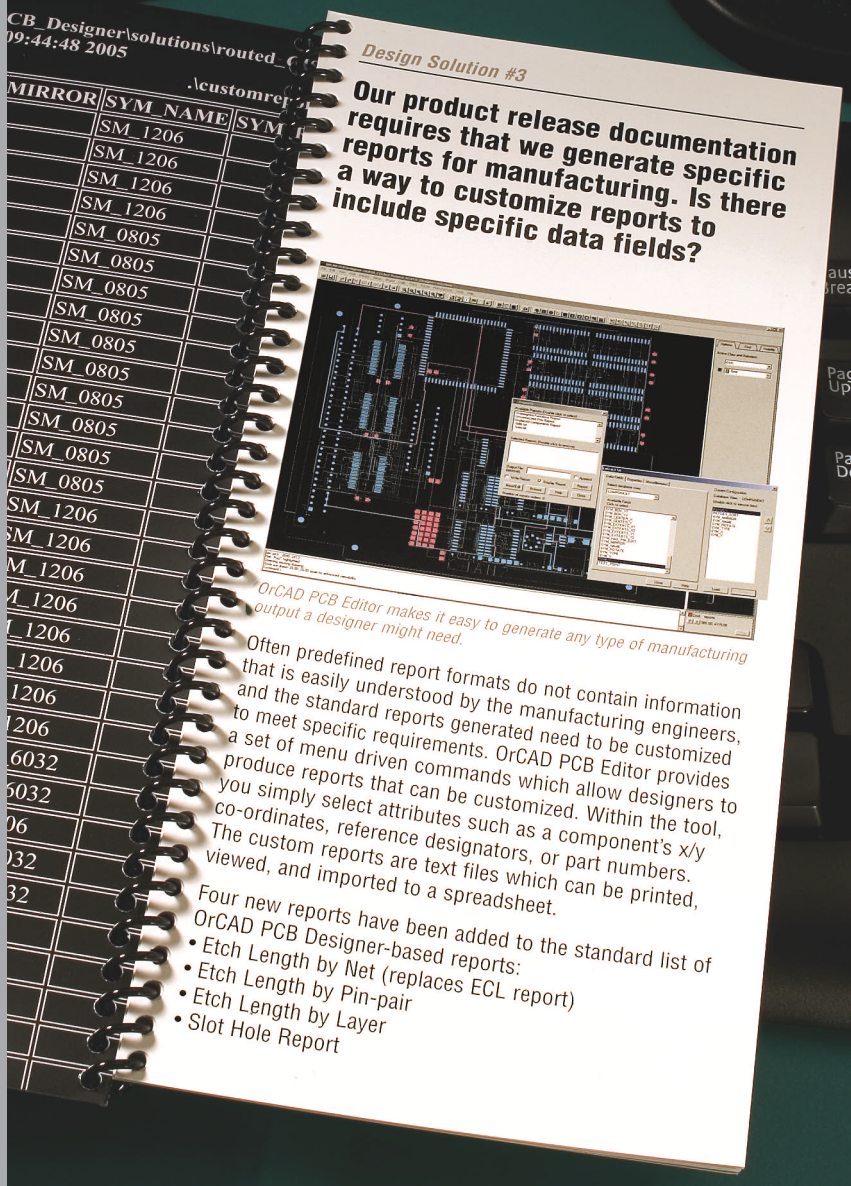

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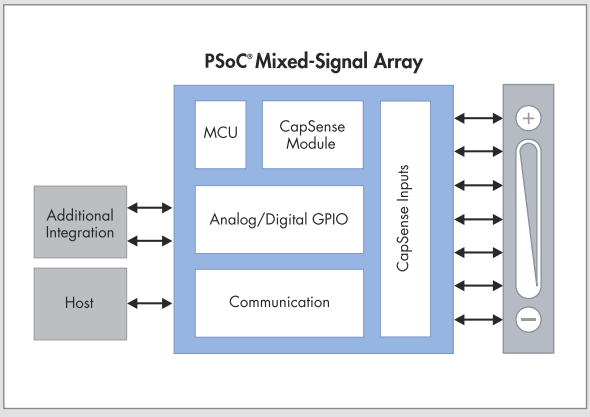
- *Easy-to-use PSoC tools provide system-level embedded design with quick time-to-market*

FOR MORE INFORMATION

For a free online or face-to-face seminar with PSoC CapSense experts, visit www.cypress.com/touch

CYPRESS CAPSENSE CIRCUIT DIAGRAM



PSoC® CapSense implementation with two buttons and a slider using a single PSoC device.

CapSense Device Selector Guide

Device	Resources	Available Package
CY8C21x34	8 KB Flash, 512 B RAM, I²C, SPI	16-SOIC, 20-SSOP, 28-SSOP, 5x5 mm 32-MLF
CY8C24x94	16 KB Flash, 1 KB RAM, I²C, Full-speed USB, SPI	8x8 mm 56-MLF

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